Development of New Multilevel Current-Source Inverter Using Inductor Cell

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1. Introduction

This paper proposes a new topology of a multilevel current-source-inverter (CSI) applying inductor cell circuit. Using this topology, smaller distortion of the inverter output current is achieved by increasing the level number of the output current as well as connecting more inductor cell circuits. The inductor cell circuit functions to obtain an intermediate current level of the multilevel output current waveform. A five-level inverter configuration is tested by using computer simulation to test the proposed multilevel current-source inverter circuit.

2. System Configuration

Fig. 1 presents the general circuit configuration of the proposed multilevel current-source inverter. The main circuit is a three-level inverter with all power switches are connected at a common potential level and the auxiliary circuits are connected in parallel with the main circuit. The chopper circuit works to generate the input current of the inverter. The auxiliary circuit is an inductor cell connected in parallel with the main three-level inverter circuit. This inductor cell circuit is composed by four power switches with blocking diodes and an inductor in the center of the circuit. This circuit functions to obtain the intermediate current level of the multilevel output current waveform by controlling the charging and discharging operation modes of the inductor cell.

Fig. 2 shows the configuration of a five-level current-source inverter circuit composed by chopper circuit, three-level inverter and a single inductor cell circuit. The operation mode of the five-level current generation is shown in Fig. 3(a) to 3(e). The chopper circuit is represented by two identical DC current sources.

Fig. 4 shows the controller diagram of the five-level inverter circuit. PI regulators are used to control the input current, I_1 and I_2, flowing through the input inductors, L*in*. Hysteresis current control is applied to regulate the current flowing through the inductor cell (I_{Lc}).

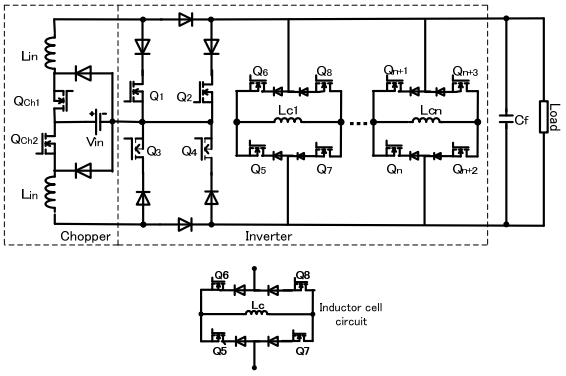


Fig. 1. Proposed multilevel current-source inverter circuit

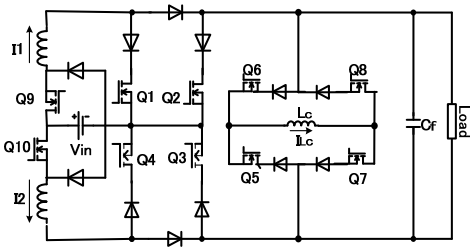
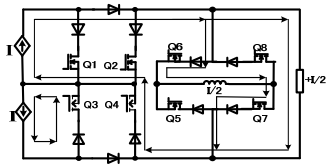
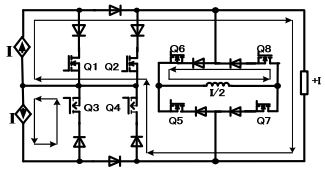


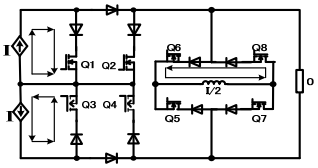
Fig. 2. Five-level current-source-inverter circuit.



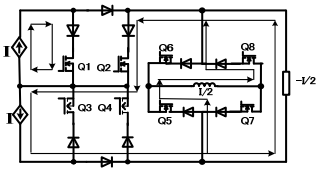
(a) Switching combination for +I/2 current generation.



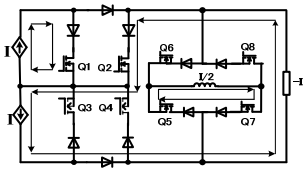
(b) Switching combination for +I current generation.



(c) Switching combination for zero current generation.



(d) Switching combination for -I/2 current generation.



(e) Switching combination for -I current generation.

Fig. 3. Operation modes of five-level CSI

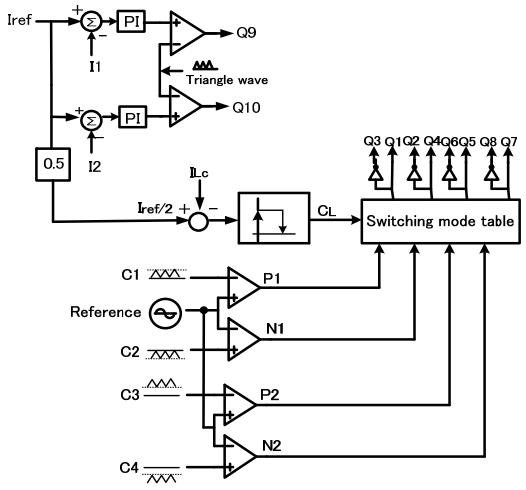


Fig. 4. Controller block diagram of five-level CSI

Table 1. Switch state of five-level inverter

Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Output
0	0	1	1	1	0	1	0	$+I$
0	0	1	1	0	1	0	1	$+I$
0	0	1	1	0	1	1	0	$+I/2$
1	0	0	1	1	0	0	1	$+I/2$
1	0	0	1	1	0	1	0	0
1	0	0	1	0	1	0	1	0
1	0	0	1	0	1	1	0	$-I/2$
1	1	0	0	1	0	0	1	$-I/2$
1	1	0	0	1	0	1	0	$-I$
1	1	0	0	0	1	0	1	$-I$

A carrier based sinusoidal modulation technique is applied to obtain a pulse width modulation (PWM) output current waveform. Table 1 lists the switch states of five-level inverter circuit for five-level current generation.

3. Simulation Results

In order to examine the proposed inverter circuit configuration, a five-level inverter topology is tested with a computer simulation. The simulation circuit specifications are listed in Table 2. Fig. 5 shows the main waveforms of proposed five-level inverter circuit. The inverter circuit generates a perfect five-level output current .It can be seen that the load current is a perfect sinusoidal waveform with small distortion. The amplitude of the inductor cell current is 5 A, i.e., half of the main input inductor current, 10 A. Fig. 6 shows the harmonics profile of three-level and five-level current using the same simulation parameters. As it can be seen, the five-level current has lower amplitude of the harmonics components. The total harmonic distortion (THD) values are 9.1% and 3.8% for the three-level and five-level current waveforms, respectively.

4. Conclusion

A new configuration of a multilevel current-source-inverter circuit has been proposed and tested in a computer simulation. The simulation results of the five-level output current shows possibility of the proposed inverter topology.

Table 2. Simulation parameters.

Input inductor (L*in*)	0.5 mH
Inductor cell (L*c*)	0.2 mH
Switching frequency	20 kHz
Filter capacitor (C*f*)	5 μF
Load	R_L = 10 Ω , L_L = 3 mH

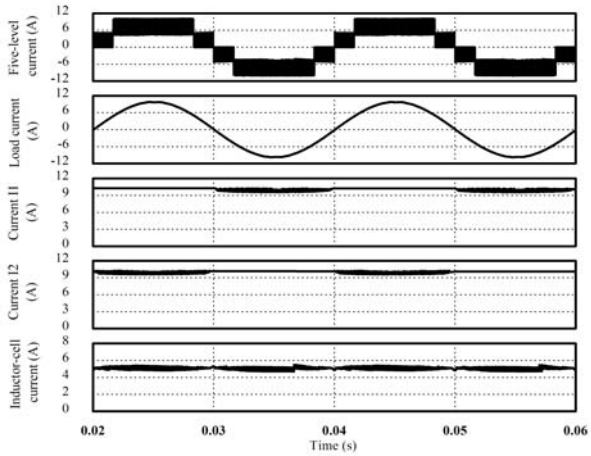


Fig. 5. Five-level current, load current, input inductor current and inductor cell current waveforms

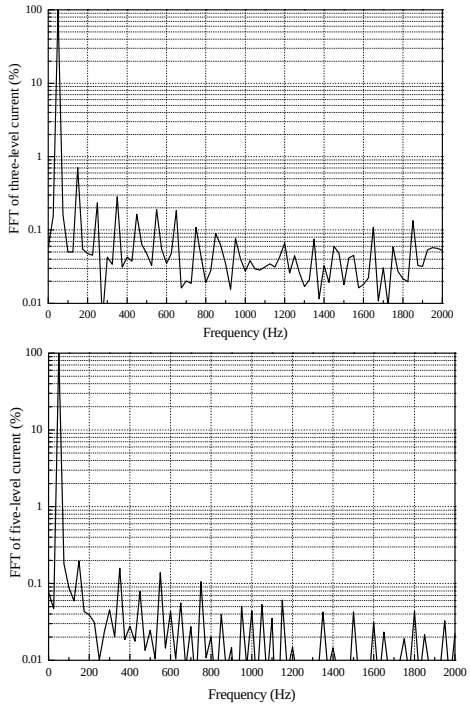


Fig. 6. Harmonic profile of three-level and five-level current waveform

References

(1) T. Noguchi, Y.Nozuki, and Suroso, "Discussion on Novel Topologies of Multi-level Power Converter Based on Duality", IEE-Japan Tech. Meet., SPC-08-89 (2008) (in Japanese).