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Space Vector Modulation of Dual Inverter with Battery and Capacitor across DC Buses

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***Abstract*-A space vector modulation (SVM) technique of a dual inverter system feeding a three-phase motor with open-end-windings is proposed in the paper, where one of the inverters has a battery power source and the other has a capacitor across the DC bus. The SVM must be achieved both to operate the motor with field-oriented control and to control the capacitor voltage at a half value of the battery by using redundant switching states at the same time. The control of the capacitor voltage is carried out by alternating a charging or a discharging mode in each switching state, taking relative phase angle between the motor voltage vector and the motor line current vector into account. In other words, it is necessary to select an optimal switching state among various redundant states which makes the capacitor voltage follow its command properly, considering the instantaneous motor power factor. The paper demonstrates an experimental setup and test results as well as computer simulation results.**

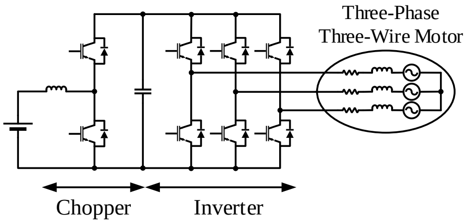

Fig. 1. Conventional motor drive with single inverter.

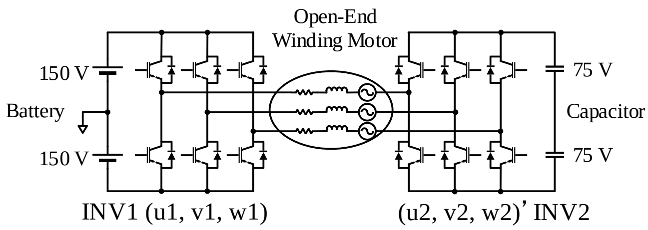

Fig. 2. Open-end winding motor drive with dual inverter system.

I. INTRODUCTION

In recent years, mileage improvement and autopilot technologies are focused on, aiming at further reduction of carbon dioxide emission of hybrid vehicles. Many of the current hybrid vehicles are based on the combination of a bidirectional chopper and a two-level inverter, and drive a high-voltage permanent magnet (PM) motor. Therefore, the line-to-line voltage of the motor is a three-level waveform with high d*v*/dt, which may cause deterioration of the total harmonic distortion (THD), conduction noise, and radiation noise. The current system has a drawback from the viewpoint of the failsafe because the motor can no longer be operated if a failure should happen in either the chopper or the inverter. In order to solve the problem above, a dual inverter system is discussed in the paper, which drives the motor with open-end windings [1]-[4].

The dual inverter technique makes it possible to generate multilevel voltage waveforms across the motor winding terminals, and has an advantage of the failsafe by replacing one of the inverter DC bus with a capacitor. In the case, it is required to generate the multilevel voltage waveforms simultaneously with controlling the capacitor voltage at a constant value [5] [6]. Particularly, it is dispensable to take the instantaneous motor power factor into account for the capacitor voltage control, i.e., charging or discharging control of the capacitor. In the paper, a novel strategy of the space vector modulation (SVM) for the dual inverter system to generate the multilevel voltage waveforms across the open-end windings of the PM motor, which allows regulating the capacitor voltage according to the instantaneous motor power factor. The proposed technique is examined through several computer simulations and experimental tests [7]. In addition, it is pointed out in the paper that the dead time detrimentally affects generation of the multilevel voltage waveforms.

II. CONFIGURATION OF DUAL INVERTER SYSTEM

A. Circuit Configuration of Dual Inverter System

Fig. 1 shows the conventional system composed of a single two-level inverter driving a three-phase PM motor with a neutral point inside of the motor. Fig. 2 is a circuit diagram of a dual inverter system, which drives an open-end winding PM motor. One inverter on the left hand side is called INV 1 and the other on the right hand side is INV 2 whose DC-bus power sources are replaced with capacitors. Each leg of the both inverters is complementary operated, and the combination of the switching states is expressed as (u1, v1, w1) (u2, v2, w2)', where the switching states "1" and "0" mean that the upper arm is turned on and off, respectively.

It is possible in the dual inverter system to generate the multilevel voltage waveforms by adding or subtracting one inverter voltage to/from the other inverter voltage. The system has a drawback of increase of the inverter counts and their DC-bus power sources, but does not require any voltage boost power converter such as the bidirectional chopper. The multilevel voltage wane form generation is expected to

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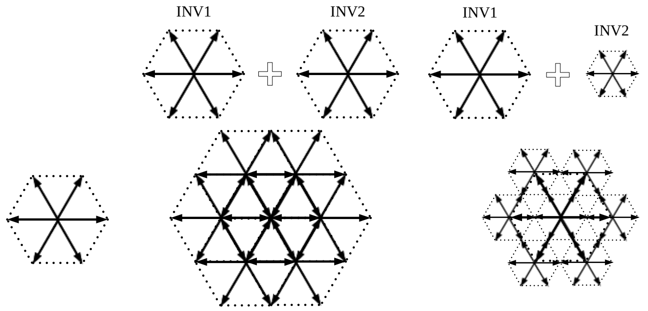
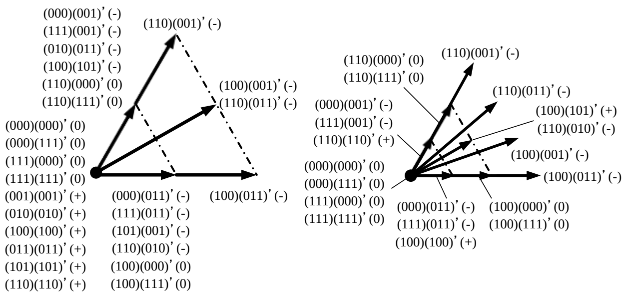


(a) Single inverter. (b) Dual inverter with 1:1 DC-bus voltage. (c) Dual inverter with 2:1 DC-bus voltage.

Fig. 3. Output voltage vectors of three systems.



(a) Dual inverter with 1:1 DC-bus voltage. (b) Dual inverter with 2:1 DC-bus voltage.

Fig 4. Relationship between DC-bus voltage ratio of dual inverter system and switching state redundancy.

improve the THD resulting in the copper loss and iron loss reductions, and to reduce the conduction noise and the radiation noise owing to the reduction of d*v*/dt. There is redundancy in the switching states of the dual inverter system. In other words, a particular voltage vector can be applied to the motor by selecting different switching modes, which allows operation of the motor with controlling the capacitor voltage of INV2. Therefore, the dual inverter system can continue to drive the motor even if one of the batteries is in failure because the switching state redundancy makes it possible to keep the capacitor voltage on the failure side at constant value and to achieve continuous operation of the motor. In addition, even in the case of the failure in one switching device of either inverter, the system can continue to operate the motor as a single inverter drive by shorting the three-phase windings with normal condition arms of the fail inverter.

B. DC-Bus Voltages and Switching State Redundancy

The dual inverter system discussed in the paper controls the INV 2 capacitor voltage at half of the INV 1 DC-bus battery voltage. The reason is to utilize the switching state redundancy and simultaneous control of the capacitor voltage and the SVM.

Fig. 3 shows output voltage vectors that the single inverter, the dual inverter system with 1:1 DC-bus voltage ratio, and the dual inverter system with 2:1 DC-bus voltage ratio, respectively. As can be seen in Fig. 3 (a), the single inverter can output 8 voltage vectors, i.e., 2 and 6 of them are zero-voltage vectors and non-zero voltage vectors, respectively. As Figs. 3 (b) and (c) show, the output voltage vectors of the dual inverter system are sum of the output voltage vectors of the two inverters. Fig. 4 illustrates the output voltage vectors from 0 to 60 deg. of the two dual inverter systems whose DC-bus voltage ratios are 1:1 and 2:1, respectively. In the figure, the capacitor charging, holding, and discharging modes are noted as "+," "0," and "–" after the switching states, respectively.

It is found from Fig. 4 that a particular voltage vector can be applied to the motor by using different switching states, which means the both systems have switching state redundancy. Only one, however, of the capacitor charging mode or the discharging mode is available among the redundant switching states in the case of the 1:1 DC-bus voltage ratio; hence, it is impossible to switch over redundantly the charging mode and the discharging mode. On the other hand, the dual inverter system with the 2:1 DC-bus voltage ratio has both of the charging mode and the discharging mode in the redundant switching states to output a particular voltage vector. This makes it possible to achieve the multilevel voltage waveform generation on the basis of the SVM and the capacitor voltage control at the same time, which is the reason why the 2:1 DC-bus voltage ratio has been employed for the dual inverter system. However, the longest voltage vectors that configure the most outer hexagon do not have the redundancy even if the 2:1 DC-bus voltage ratio is employed, so the longest voltage vectors are not utilized in the SVM discussed in the paper.

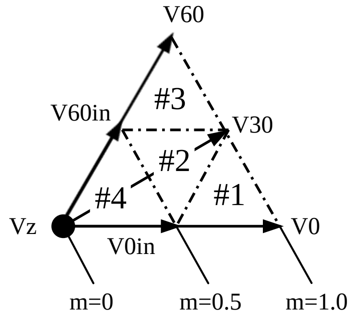


Fig. 5. Voltage vectors used in SVM and modulation index.

III. SELECTION OF VOLTAGE VECTORS IN SVM

Fig. 5 illustrates the voltage vectors whose phase angle is from 0 to 60 deg., for example, where m denotes a modulation index. The modulation index m = 1.0 when the circular locus of the voltage vector generated by the SVM is inscribed in the outer hexagon, and m = 0.5 when the locus is inscribed in the inner hexagon.

The SVM is carried out by synthesizing some discrete inverter voltage vectors at appropriate ratio to output a commanded voltage vector with an arbitrary phase angle and an arbitrary norm. The commanded voltage vector can be synthesized by using three voltage vectors surrounding the commanded voltage vector in a triangle shape. In the case of the #1 triangle sector, for example, the three voltage vectors V0, V0in, and V30

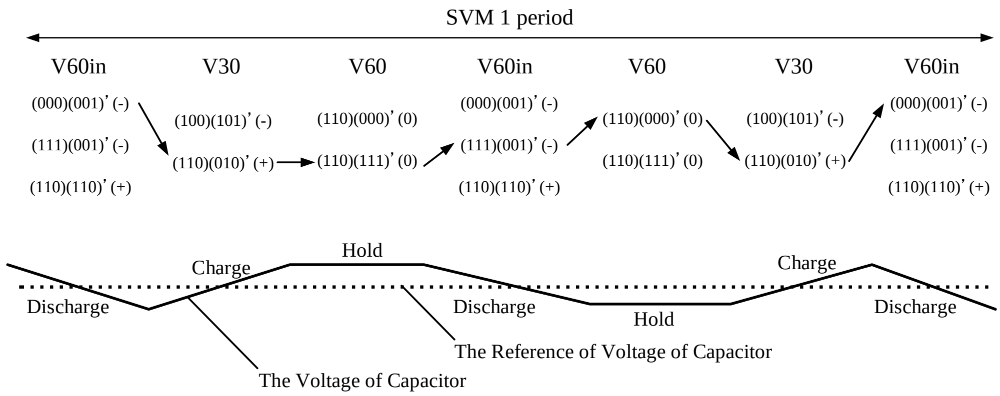


Fig. 6. Simultaneous control of multilevel voltage waveform generation with SVM and Capacitor voltage.

surrounding the corresponding triangle sector are used for the SVM to synthesize the commanded voltage vector, which contributes to reduce the d*v*/dt. The triangle sectors from #1 to #3 do not use zero-voltage vectors Vz for the SVM, resulting in 9-level voltage waveforms across each motor winding, but Vz must be used in the sector #4.

IV. Capacitor Voltage Control and Instantaneous Motor Power Factor

A. Capacitor Voltage Control of INV 2

The DC-bus voltage sources of INV 2 are replaced with the capacitors in the dual inverter system of the paper. The voltage across the capacitor must be controlled to keep a constant value by charging and discharging it, and multilevel voltage waveform generation must also be achieved at the same time.

The dual inverter system has redundant switching states, and can output a particular voltage vector with different redundant switching states as described previously. Polarity of the current flowing into the capacitor changes according to the capacitor charging mode or the discharging mode specified by every switching state. As illustrated in Fig. 6, the multilevel voltage waveform generation with the SVM and the capacitor voltage control can simultaneously be carried out by selecting an appropriate switching state among the redundant states. It should be noted that almost unity power factor is assumed as an operating condition of the motor in the example illustrated in Fig. 6.

B. Impact of Instantaneous Motor Power Factor

Fig. 7 shows a relationship between the motor line current vector and the polarities of the motor line currents, where the polarity signs indicate the current directions in the motor windings, i.e., "+" means a direction from INV 1 to INV 2, while "–" does the opposite direction. The capacitor charging mode or the discharging mode can be determined by the current direction of the motor windings in every switching state.

It is, however, assumed that the PM motor is connected to the dual inverter system as a load, which is inherently an inductive load; thus, the motor line currents lag behind the voltage vector generated by the SVM. Each line current

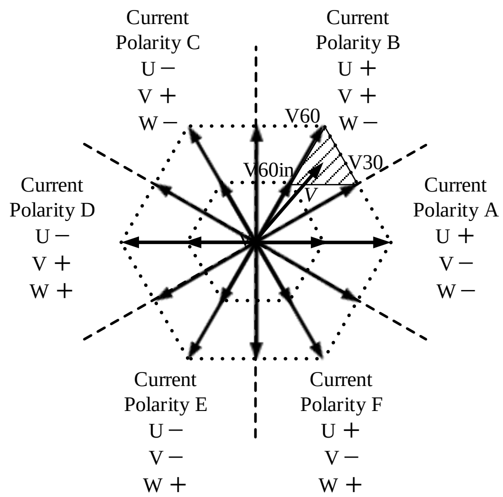


Fig. 7. Relationship between current vector and motor line currents.

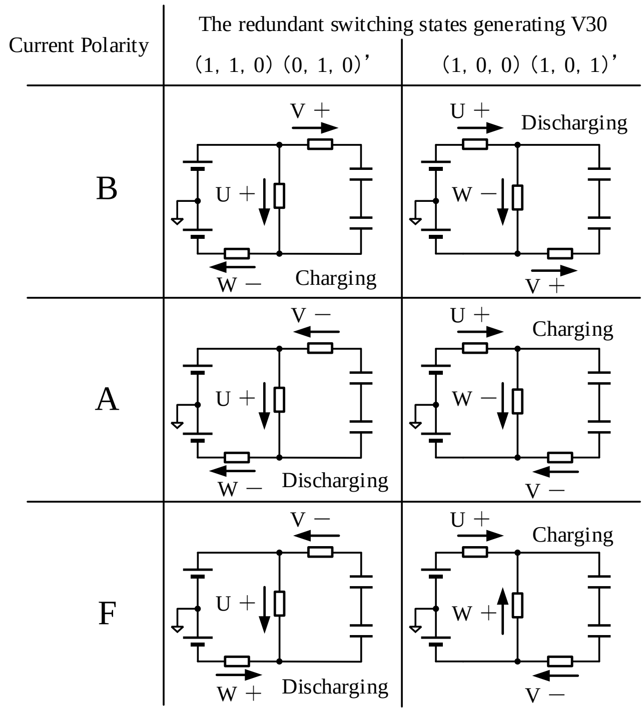


Fig. 8. Relationship between redundant switching states to output V30 and capacitor voltage control modes.

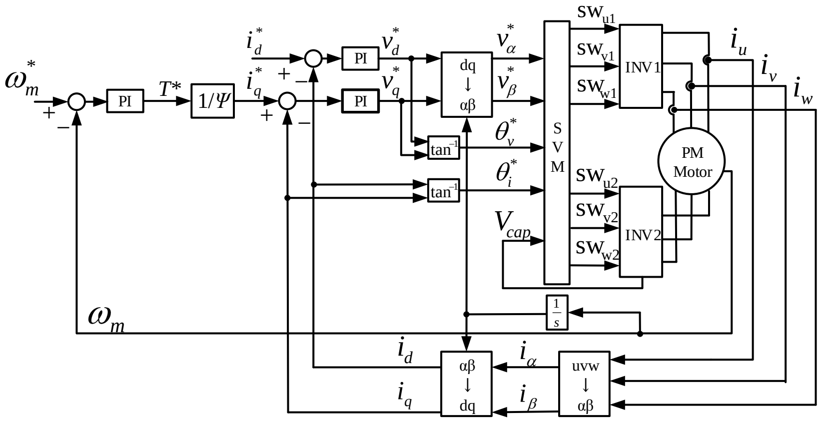


Fig. 9. Control block diagram of dual inverter system for open-end winding PM motor drive.

TABLE I. COMPUTER SIMULATION CONDITIONS.

Switching frequency		10 kHz
Voltage of battery (INV1)		300 V
Voltage of capacitor (INV2)		150±5 V
Capacitance of capacitor (INV2)		1320 μF
Motor speed command value		10000 r/min
Dead time		0 μs
Motor parameters	Number of poles	2
	Number of flux linkage	0.1 Wb
	Moment of inertia	0.0001 kgm^2
	Damping coefficient	0.002 N/rad/s
	Phase resistance	1 Ω
	Phase inductance	5 mH

direction changes according to the instantaneous motor power factor, which may be affected by the motor operating conditions and the motor parameters. This implies that the instantaneous motor power factor must be taken into account to control the capacitor voltage at a constant value.

Let's assume the case where the commanded voltage vector is in the hatched sector as illustrated in Fig. 7. The available voltage vectors are V60, V60in, and V30 to synthesize the commanded voltage vector in the case. The maximum lagging phase angle between the voltage and the current vectors is 90 deg., which means that the current direction is in one of "B," "A," and "F." Two of the redundant switching states to generate V30 voltage vector are shown in Fig. 8, for example, where the relationship between the motor line current direction and the capacitor charging or the discharging mode. A switching state (110)(010)' makes the motor line current charge the capacitor in the case of the current vector direction "B," but the identical switching state makes the capacitor discharging mode in the case of the current vector direction "A" or "F." In general, the relationship between the switching state and the capacitor charging or discharging mode cannot uniquely be determined if the motor line current vector phase angle changes due to the instantaneous motor power factor. Therefore, it is indispensable for the SVM process to choose an appropriate switching state among the redundant switching states that

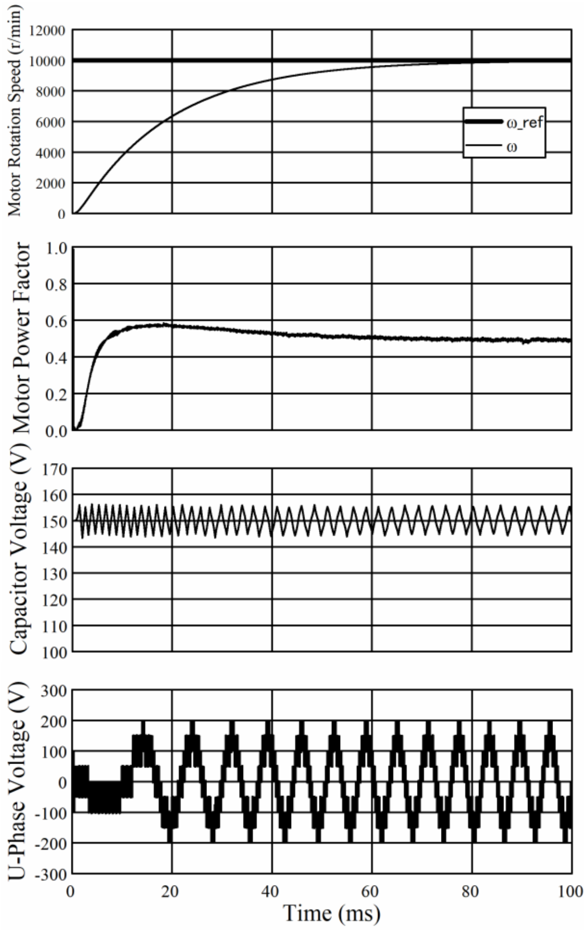


Fig. 10. Simulation results.

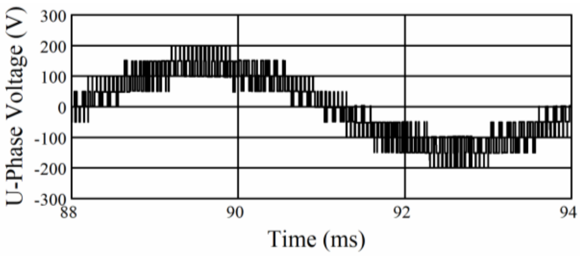


Fig. 11. Expanded waveform of voltage across phase U winding terminals.

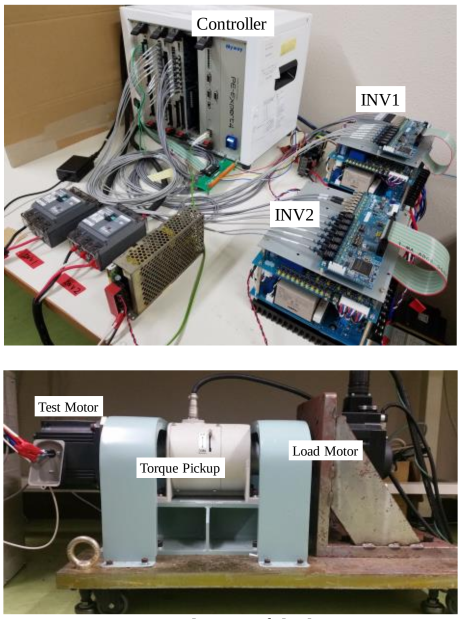


Fig. 12. Experimental setup of dual inverter system.

TABLE II. EXPERIMENT TEST CONDITIONS.

Switching frequency		10 kHz
Voltage of battery (INV1)		300 V
Voltage of capacitor (INV2)		150±5 V
Capacitance of capacitor (INV2)		1320 μF
d-axis current command value		0 A
q-axis current command value		1 A
Motor speed		1100 r/min
Dead time		4 μs
Motor parameters	Number of poles	8
	Rated power	1000 W
	Rated speed	2000 r/min
	Rated torque	4.78 Nm
	Rated current	3.7 A
	Armature resistance	1.1 Ω
	Number of flux linkage	0.174 Wb
	d-axis inductance	11.0 mH
	q-axis inductance	25.0 mH

makes it possible to control the capacitor voltage at a constant value according to the instantaneous motor power factor.

V. COMPUTER SIMULATION AND RESULTS

Some computer simulations have been conducted to examine the basic operation of the dual inverter system feeding the open-end winding PM motor, where the capacitor is installed across the DC bus of INV 2 and the proposed control technique is introduced into the system. The control block diagram is indicated in Fig. 9. The motor is controlled with a field-oriented control (vector control) algorithm, so has a speed control loop and a current control loops in the controller. The phase angle between the voltage vector and the motor line current vector is calculated on the synchronously rotating (*d*-*q*) reference frame, and is utilized to select the most appropriate switching state among the redundant switching states, as well as the feedback value of the capacitor voltage of INV 2.

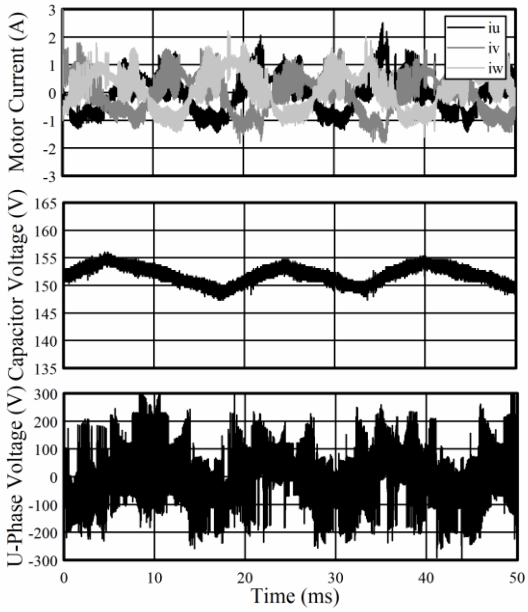


Fig. 13. Experimental test result.

TABLE I and Fig. 10 show the simulation conditions and the operation waveforms obtained through the simulations, respectively. The motor speed, the instantaneous motor power factor, the capacitor voltage, and the voltage across the phase U winding terminals are shown from the top to the bottom of Fig. 10. As can be seen in the figure, even though the dynamic variation of the instantaneous motor power factor is caused by a transient acceleration of the motor speed, the capacitor voltage is properly kept constant at 150±5 V. Fig. 11 is an expanded waveform of the motor winding voltage, where the 9-level voltage waveform is also properly observed.

VI. EXPERIMENTAL SETUP AND TEST RESULTS

Experimental tests have been conducted with an experimental setup of the dual inverter system as shown in Fig. 12. The open-end winding PM motor is controlled by a field-oriented control (vector control) algorithm, and its speed is regulated at 1100 r/min by a load servo motor directly connected to the test motor. The rated output power of the test motor is 1 kW, and is fed by the two 5-kVA inverters in which one of the inverter has only the capacitor across the DC bus. Experimental test conditions are listed in TABLE II, and the test result is shown in Fig. 13. As shown in the test result, the multilevel voltage waveform is generated across the open-end winding of the test motor, but contains a lot of unexpected noise pulses in the waveform, which detrimentally deteriorates the THD of the voltage waveform. However, the three-phase line currents are balanced and include less harmonic components than the fundamental components. In addition, the capacitance voltage is properly controlled to be around 150 V within the specified hysteresis band. All in all, therefore, the proposed approach woks well, but must be improved to compensate for the unexpected voltage pulses in the output multilevel voltage waveforms.

VII. Discussion on Impact of Dead Time

Particular switching sequences are included on the dual inverter system with the 2:1 DC-bus voltage ratio described so far, which synchronously turns on or turns off the switching devices in the same phase of the both inverters. As shown in Fig. 14, for example, let's assume the transition from a switching state "A" to "B", where the upper arms of the both inverter are turned on in "A," while the both lower arms are on in "B." Since the switching state during the dead time is determined by the line current direction, the error voltage vector is generated because the switching state during the dead time is "0" and "1." In other words, it is difficult to avoid such an unexpected switching state during the dead time because the switching state "A" cannot directly be changed to "B" due to the dead time. Fig. 15 shows an example of the unexpected error voltage generated during the dead time. If the commended voltage vector is located in the specific hatched sector, the three- voltage vectors V60, V60in, and V30 are used for the SVM. Although the proper switching sequence is V60in → V30 → V60 → V60 in → ···, the unexpected irregular voltage vectors such as V120in, V0, and Vz are inserted in every transition of the switching states. However, the conventional single inverter and the dual inverter system with the 1:1 DC-bus voltage ratio do not have this problem because there are not transitions that require synchronous turning on or turning off of the same phase switching devices in the both inverters.

The dead time is indispensable to prevent the DC bus of the inverters from the short circuit. Therefore, elimination of the unexpected error voltage during the dead time is important point in the dual inverter system that has the capacitors instead of the DC power source and that has the DC-bus voltage ratio of 2:1. The investigation on the technical problem is one of the future works of the authors'.

VIII. Conclusion

This paper has described an SVM technique of the dual inverter system feeding an open-end winding PM motor, where one of the DC busses in the system is replaced with capacitors. The SVM is achieved by selecting an optimal switching state among the redundant states that can generate multilevel voltage waveforms across the open-end windings and can simultaneously control the capacitor voltage at a fixed value. The paper has pointed out that the instantaneous motor power factor is important to take into account as well as the switching states of the dual inverter system.

It has also been suggested in the paper that the dead time causes unexpected error voltage pulses in the multilevel voltage waveforms, which will be investigated in detail in the future study.

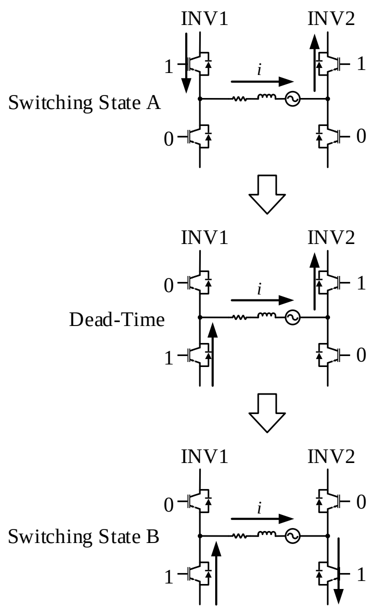


Fig. 14. Impact of dead time in simultaneous switching.

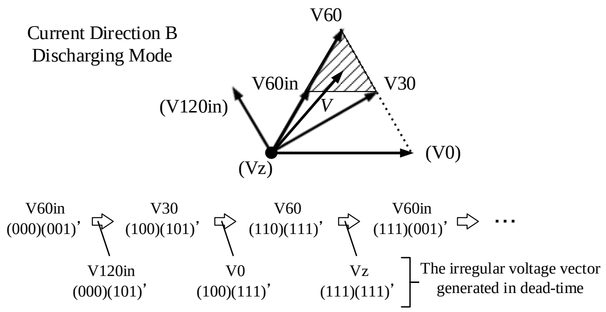


Fig. 15. Unexpected error voltages during dead time.

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