

# Compensation for Multilevel Voltage Waveform Generated by Dual Inverter System

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**Abstract**— A space vector modulation (SVM) technique of a dual inverter system feeding an open-end-winding PM motor and improvement technique of generated multi-level voltage waveforms with the system are proposed in the paper. In the proposed system, one of the inverters has a battery power source and the other has a capacitor across the DC-bus. The SVM must be achieved both to generate multilevel voltage waveforms to the motor and to control the capacitor voltage constantly at the same time by using redundant switching states of the system. In order to control the capacitor voltage, it is necessary to select the optimal switching state with SVM considering the instantaneous motor power factor. In addition, it is also necessary to eliminate error voltage vectors contained in outputted multilevel voltage waveform. The error voltage vectors are generated during the dead time when the switching devices in the same phase of both inverters are synchronously turned on or turned off. Therefore, the special dead time technique is need for the SVM of the dual inverter system. The paper demonstrates proposed SVM techniques through computer simulation and experimental tests.

**Keywords**—Dual inverter system, space vector modulation, open-end-winding motor, capacitor voltage control, dead time

## I. INTRODUCTION

In recent years, mileage improvement and autopilot technologies are focused on to reduce carbon dioxide emission of hybrid vehicles. Many of the current hybrid vehicles are based on the combination of a bidirectional chopper and a two-level inverter, and drive a high-voltage permanent magnet (PM) motor. Therefore, the line-to-line voltage of the motor is a three-level waveform with high  $dv/dt$ , which may cause deterioration of the total harmonic distortion (THD), conduction noise, and radiation noise. The current system also has a drawback from the viewpoint of the failsafe because the motor cannot be operated if either the chopper or the inverter is failed. In order to solve the problems above, a dual inverter system which drives open-end-winding motor with two inverters is researched. In the conventional dual inverter system, the both inverters have a battery power source across the DC-bus and the battery voltages are same value [1]. On the other hand, one of the battery power source across the DC-bus is replaced with capacitors and the capacitor voltage is

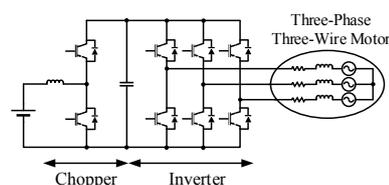


Fig. 1. Conventional motor drive by single inverter system.

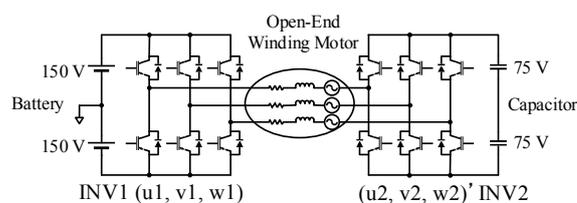


Fig. 2. Open-end winding motor drive by dual inverter system.

controlled at a half value of the other hand battery voltage in the proposed dual inverter system [2][3]. In the case, it is required both to control the capacitor voltage at commanded value and to generate multilevel voltage waveform to the open-end-winding motor terminals at the same time. Particularly, it is indispensable to take the instantaneous motor power factor into account for the capacitor voltage control, i.e., charging or discharging control of the capacitor. The proposed space vector modulation (SVM) technique makes it possible to achieve both to capacitor voltage control and multilevel voltage waveform generation at the same time [4]. However, the outputted multilevel voltage waveforms with proposed system contain a lot of unexpected error voltage pulses, which are generated during the dead time when the both switching devices in the same phase are synchronously turned on or turned off [5]. The measure to improve the multilevel voltage waveforms is proposed, however, this is incomplete because it doesn't consider the fluctuation of switching speed due to the motor current norm [6]. In the paper, a novel strategy of the SVM for the dual inverter system is proposed, which allows the capacitor voltage control and the multilevel voltage waveform generation at the same time according to the instantaneous motor power factor. Furthermore, the compensation for synchronous switching of dual inverter system is also proposed in this paper, and the above SVM techniques are examined through several experimental tests.

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## II. CONFIGURATION OF DUAL INVERTER SYSTEM

### A. Circuit Configuration of Proposed Dual Inverter System

Fig. 1 shows the conventional motor drive system with a single two-level inverter which drives a three-phase PM motor with a neutral point inside of the motor. Fig. 2 is a circuit diagram of the proposed dual inverter system with two single two-level inverters which drives an open-end-winding PM motor. The left-hand side inverter is called INV 1 and the other on the right-hand side is INV 2 whose DC-bus battery power sources are replaced with capacitors. Each leg of the both inverters is complementary operated, and the combination of the switching states is expressed as  $(u1, v1, w1)$   $(u2, v2, w2)$ , where the switching states “1” and “0” mean that the upper arm is turned on and off, respectively.

The dual inverter system can generate the multilevel voltage waveforms by adding or subtracting one inverter output voltage to/from the other inverter output voltage. The system has a drawback of increasing the inverter counts and their DC-bus battery power source counts, but does not require any voltage boost power converter such as the bidirectional chopper. The multilevel voltage waveform generation is expected to improve the THD resulting in the copper loss and iron loss reductions, and expected to reduce the conduction noise and the radiation noise owing to the reduction of  $dv/dt$ . The dual inverter system has the redundancy in the switching states. In other words, a particular voltage vector can be applied to the motor with different several switching states, which allows operation of the motor with controlling the capacitor voltage of INV 2. If capacitors are connected in parallel to the batteries across both side inverter DC-buses respectively, the dual inverter system can continue to drive the motor even if one of the batteries is in failure. Because the switching state redundancy makes it possible to keep the capacitor voltage on the failure side at constant value and to achieve continuous operation of the motor as the dual inverter drive as shown in Fig. 2. In addition, in the case of the failure in one switching device of either inverter, the system can continue to operate the motor as a single inverter drive by shorting the three-phase windings with normal condition arms of the fail inverter. In this way, the proposed dual inverter system has advantages of failsafe.

### B. DC-Bus Voltage Ratio and Switching State Redundancy

The dual inverter system discussed in the paper controls the capacitor voltage of INV 2 at half of the INV 1 DC-bus battery voltage. The reason is, in addition to generate the 9-level voltage waveform, to utilize the switching state redundancy.

The single inverter can output 8 voltage vectors, i.e., 2 and 6 of them are zero-voltage vectors and non-zero voltage vectors, respectively. The output voltage vectors of the dual inverter system are sum of the output voltage vectors of the two inverters. Fig. 3 shows the output voltage vectors from 0 to 60 deg. of the two dual inverter systems whose DC-bus voltage ratios are 1:1 and 2:1, respectively. In the figure, the capacitor charging, holding, and discharging modes are noted as “+,” “0,” and “-” after the switching states, respectively. As shown in Fig. 3, a particular voltage vector can be applied to the motor by using different several switching states, which means the

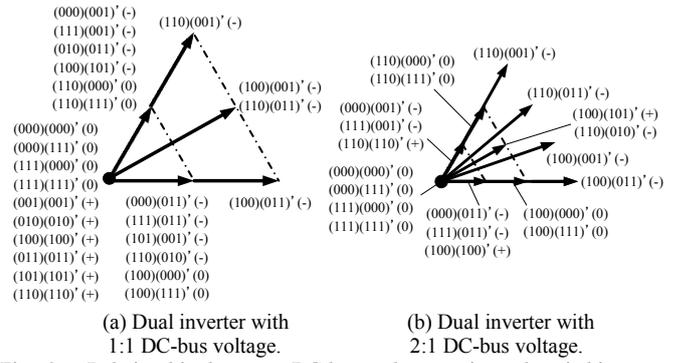


Fig. 3. Relationship between DC-bus voltage ratio and switching state redundancy.

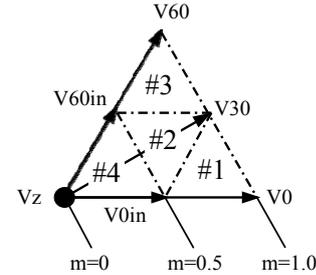


Fig. 4. Voltage vectors used in SVM and definition of modulation index.

both systems have the switching state redundancy. However, only one of the capacitor charging mode or the discharging mode is available among the redundant switching states in the case of the 1:1 DC-bus voltage ratio; hence, it is impossible to switch over the charging mode and the discharging mode redundantly. On the other hand, there is both of the charging mode and the discharging mode in the redundant switching states of the dual inverter system with the 2:1 DC-bus voltage ratio. This makes it possible to control the capacitor voltage and simultaneously to generate multilevel voltage waveform, which is the reason why the 2:1 DC-bus voltage ratio has been employed for the proposed dual inverter system. However, the longest voltage vectors that configure the most outer hexagon do not have the redundancy even if the 2:1 voltage ratio is employed, so the longest voltage vectors are not utilized in the SVM discussed in the paper.

## III. SELECTION OF VOLTAGE VECTORS IN SVM AND DEFINITION OF MODULATION INDEX

Fig. 4 illustrates the voltage vectors from 0 to 60 deg. of dual inverter system employed 2:1 DC-bus voltage ratio, where the symbol “ $m$ ” denotes a modulation index. The modulation index is defined as  $m = 1.0$  when the circular locus of the voltage vector generated by the SVM is inscribed in the outer hexagon and  $m = 0.5$  when the locus is inscribed in the inner hexagon. As shown in Fig. 3., the system can generate a longer voltage vector than  $m = 1.0$  by using the longest voltage vectors which configure the most outer hexagon, however, the longest vectors do not have a switching redundancy, i.e., it cannot operate capacitor voltage with SVM. Therefore the modulation index  $m = 1.0$  is defined as above, where the capacitor voltage control is achieved with SVM.

The SVM is carried out by synthesizing three discrete inverter voltage vectors at appropriate ratio to output a

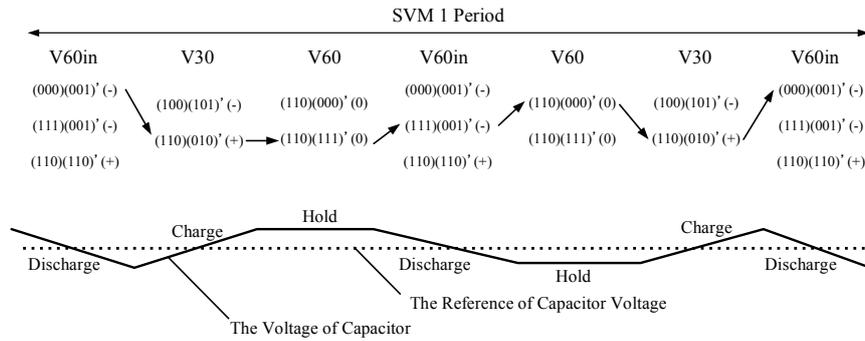


Fig. 5. Simultaneous control of multilevel voltage waveform generation and capacitor voltage with SVM.

commanded voltage vector. The commanded voltage vector can be synthesized by using three voltage vectors surrounding the commanded voltage vector in a triangle shape. For example, in the case that the commanded voltage vector is in the #1 triangle sector, the three voltage vectors  $V_0$ ,  $V_{0in}$ , and  $V_{30}$  surrounding the corresponding triangle sector are used for the SVM to synthesize the commanded voltage vector, which contributes to reduce the  $dv/dt$ . The triangle sectors from #1 to #3 do not use zero-voltage vectors  $V_z$  for the SVM, resulting in 9-level voltage waveforms across each motor winding, but  $V_z$  must be used in the sector #4.

#### IV. CAPACITOR VOLTAGE CONTROL AND IMPACT OF INSTANTANEOUS MOTOR POWER FACTOR

##### A. Capacitor Voltage Control of INV2

The DC-bus voltage sources of INV 2 are replaced with capacitors in the proposed dual inverter system of the paper. The capacitor voltage must be controlled at constant value by charging and discharging it, and simultaneously multilevel voltage waveform generation must also be achieved.

The dual inverter system has redundant switching states and can output a particular voltage vector with different several redundant switching states as described previously. The capacitor charging mode or the discharging mode changes according to polarity of the current flowing into the capacitor. As illustrated in Fig. 5, the multilevel voltage waveform generation with the SVM and the capacitor voltage control can simultaneously be carried out by selecting an appropriate switching state among the redundant states.

##### B. Impact of Instantaneous Motor Power Factor

Fig. 6 shows the relationship between the phase of motor line current vector and the polarities of the motor line currents, where the polarity signs “+” means a motor current direction from INV 1 to INV 2, while “-“ means the opposite direction. The capacitor charging mode or the discharging mode is determined by the motor line current directions in every switching state. The PM motor connected to dual inverter system is, however, inherently an inductive load; thus, the motor line currents lag behind the voltage vector generated with SVM. Each line current direction changes according to the instantaneous motor power factor, which is affected by the motor operating conditions and the motor parameters. This implies that the instantaneous motor power factor must be taken into account to control the capacitor voltage. Let’s

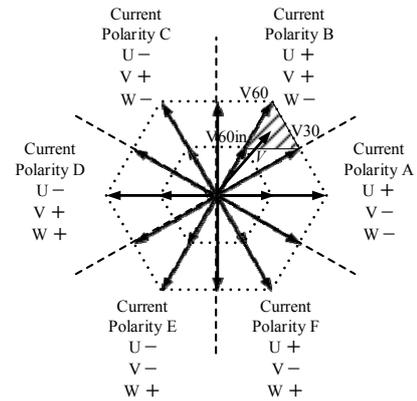


Fig. 6. Relationship between current vector phase angle and motor line currents polarity.

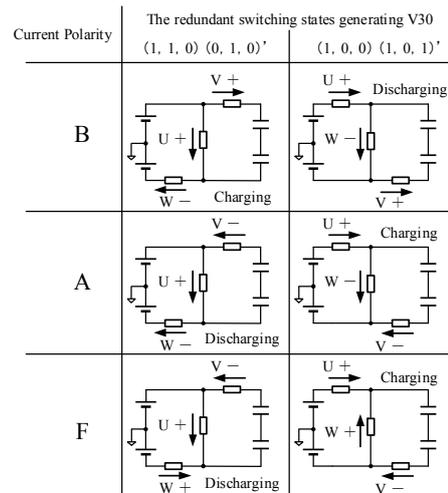


Fig. 7. Relationship between redundant switching states and capacitor voltage control modes.

assume the case that the commanded voltage vector is in the hatched sector as illustrated in Fig. 6. The three voltage vectors  $V_{60}$ ,  $V_{60in}$ , and  $V_{30}$  are used to synthesize the command voltage vector. The maximum lagging phase angle between the voltage vector and the current vector is 90 deg., which means that the current polarity is in one of “B,” “A,” and “F.” Two of the redundant switching states to generate  $V_{30}$  voltage vector are shown in Fig. 7, for example, where the relationship between the motor line current polarity and the capacitor charging or the discharging mode. A switching state (110)(010)<sup>'</sup> is the capacitor charging mode in the case of the current vector direction “B,” but the switching state is capacitor



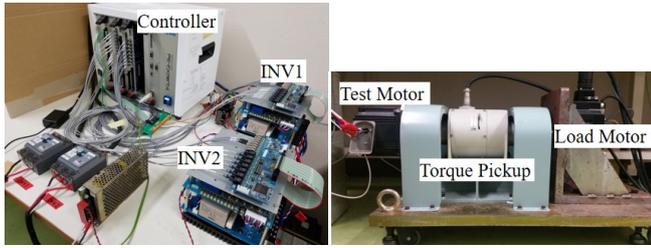


Fig. 10. Experimental setup of dual inverter system.

TABLE II. EXPERIMENT TEST CONDITIONS.

Switching frequency		10 kHz
Voltage of battery (INV1)		300 V
Voltage of capacitor (INV2)		$150 \pm 5$ V
Capacitance of capacitor (INV2)		$1329.4 \mu\text{F}$
$d$ -axis current command value		0 A
$q$ -axis current command value		1 A
Motor speed		840, 1680 r/min
Dead time		$4 \mu\text{s}$
Motor parameters	Number of poles	8
	Rated power	1000 W
	Rated speed	2000 r/min
	Rated torque	4.78 Nm
	Rated current	3.7 A
	Armature resistance	$1.1 \Omega$
	Number of flux linkage	$0.174 \text{ Wb}$
	$d$ -axis inductance	11.0 mH
	$q$ -axis inductance	25.0 mH

## VII. IMPACT OF DEAD TIME

### A. Dead Time Technique of Dual Inverter System

Particular switching sequences are included on the dual inverter system with the 2:1 DC-bus voltage ratio, where the switching devices in the same phase of both inverters are synchronously turned on or turned off. For example, let's assume the transition from a switching state "A" to "B" as shown in Fig. 12, where the upper arms of the both inverters are turned on in "A," while both lower arms are turned on in "B." Because the switching state during the dead time is determined by the line current direction, the error voltage vector is generated because the switching state of INV1 and INV2 during the dead time are "0" and "1," respectively. Fig. 13 shows an example of the unexpected error voltages inserted during each dead time. In the case of the commended voltage vector in the hatched sector, the three voltage vectors  $V_{60}$ ,  $V_{60in}$ , and  $V_{30}$  are used for the SVM. The proper switching sequence is  $V_{60in} \rightarrow V_{30} \rightarrow V_{60} \rightarrow V_{60in} \rightarrow \dots$ , however, the irregular voltage vectors such as  $V_{120in}$ ,  $V_0$ , and  $V_z$  are generated during every dead time of synchronous switching.

TABLE III shows the dead time technique of dual inverter system to eliminate unexpected irregular voltage vectors during the dead time in case of the line current direction from INV1 to INV2. The upper arms of the both inverters are turned on in state #1. The first dead time is inserted in INV2 where the line current follows into INV2 in state #2, when the upper arm of INV1 keeps turning on, and the upper arm of INV2 also keeps turning on with the diode. The second dead time starts to be inserted in INV1 where the line current follows out

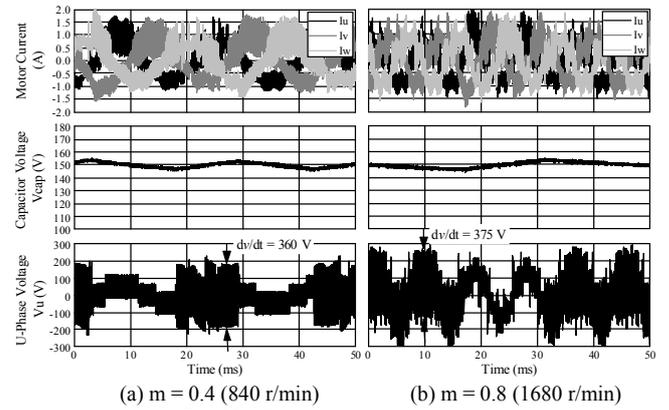


Fig. 11. Experimental test results.

immediately after the first dead time of INV2 is finished at the start of state #3. In state #3, the lower arm of INV1 turns on with the diode which is during the second dead time, and the lower arm of INV2 also turns on which is after the first dead time. After the second dead time of INV1 is finished, the lower arms of the both inverters turn on in state #4. In this way, it can synchronously turn on or turn off the switching devices in the same phase of the both inverters without error voltages.

### B. Proposed Compensation for Synchronous Switching of Dual Inverter System

However, there is a difference of the switching speed between switching devices in the same phase of INV1 and INV2; hence, it is difficult to insert the second dead time precisely at the end of the first dead time. Fig. 14 shows the difference of switching timings between INV1 and INV2 obtained through the experimental test, which means the difference is changed by the line current norm. In the figure, the positive line current indicates a direction from INV 1 to INV 2 and the negative does the opposite. Let's assume the synchronous turning off as shown in TABLE III, where the turning off time of the switching device of INV1 is expressed as  $\text{toff1}$ , the turning on time of INV2 as  $\text{ton2}$ , and the reverse recovery time of the diode of INV2 as  $\text{trr2}$ . When the synchronous switching is done and the state changes from #2 to #3, the lower arm of INV1 gets turning on with diode after the upper arm turns off with the IGBT, while the lower arm of INV2 gets turning on with the IGBT after the upper arm turns off with the diode. In this case, the switching time of INV1 is almost equal to  $\text{toff1}$  because the turning on time of the diode can be ignored for such a high speed, while the switching time of INV2 is the sum of the reverse recovery time of diode and the turning on time of IGBT, i.e.,  $\text{trr2} + \text{ton2}$ . As a result, the switching time of INV1 is longer than INV2 because the reverse recovery time of INV2 is shorter in case the line current norm is small, i.e.,  $\text{toff1} > \text{trr2} + \text{ton2}$ .

The test results employed the conventional dead time technique and the dead time technique with proposed compensation are shown in Fig. 15 and Fig. 16, respectively. It is observed that the  $\text{dv}/\text{dt}$  is reduced by 16.7 % at low modulation index ( $m = 0.4$ ) and deteriorated by 2.7 % at high modulation index ( $m = 0.7$ ) with conventional dead time technique, on the other hand the  $\text{dv}/\text{dt}$  is reduced by 30.6 % at low modulation index ( $m = 0.4$ ) and deteriorated by 4.0 % at high modulation index ( $m = 0.7$ ) with proposed dead time

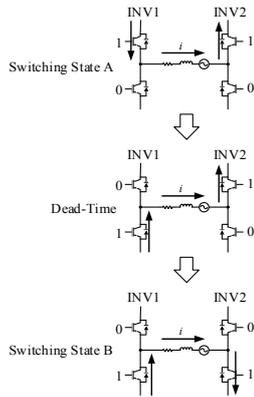


Fig. 12. Impact of dead time in synchronous switching.

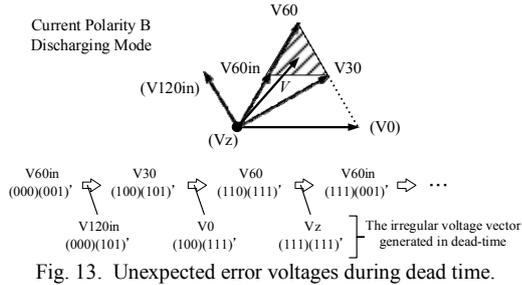


Fig. 13. Unexpected error voltages during dead time.

TABLE I. Dead time technique to eliminate error voltage vectors.

State	INV1		INV2		Phase Voltage
	Up	Un	Up	Un	
#1	1	0	1	0	Vdc1-Vdc2
#2	1	0	0	0	Vdc1-Vdc2
#3	0	0	0	1	0
#4	0	1	0	1	0

technique. Therefore, the proposed approach works well at low modulation index, but there is not remarkable improvement at high modulation index. At high modulation index, there is not only synchronous switching in the same phase of both inverters in the SVM sequence, but complicated switching transients where the switching devices in several phases in one inverter get turned on or turned off at the same time. For this reason, it is difficult to improve the multilevel voltage waveform with the above dead time technique at high modulation index.

### VIII. CONCLUSION

This paper has described SVM techniques of the dual inverter system for open-end winding PM motor drive, where one of the inverters has only capacitors across the DC-bus. The SVM is achieved to output voltage waveforms across the open-end winding terminals and simultaneously regulate the capacitor voltage at a half of the other battery voltage by selecting an appropriate switching state among the redundant states. In particular, it is indispensable for capacitor voltage control with the proposed SVM to consider the instantaneous motor power factor. This paper has also been described that the dead time causes unexpected irregular voltages in the generated multilevel voltage waveforms and proposed compensation for the conventional dead time technique. It has been verified that the dead time technique employed the proposed compensation eliminates the irregular voltage vectors in the output multilevel

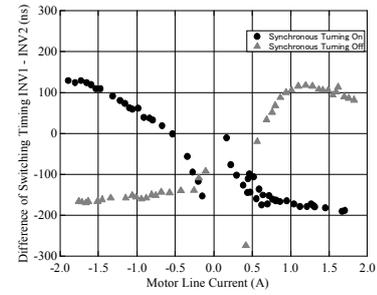


Fig. 14. Difference of switching speed between INV1 and INV2.

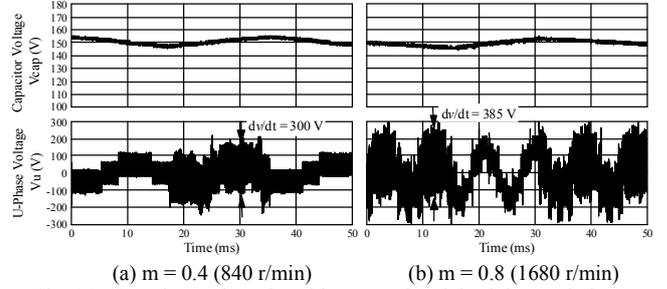


Fig. 15. Experimental results with conventional dead time technique.

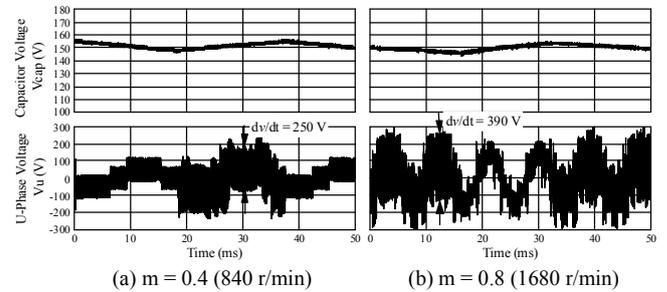


Fig. 16. Experimental results with proposed dead time technique.

voltage waveforms through experimental tests. However, the output multilevel voltage waveforms still have error voltage pulses, which will be investigated in detail in future works.

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