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Paper

Power Efficiency and Power Density Enhancement of Pure Sinusoidal Output Single-Phase Multilevel Current-Source Inverter Using Class-A Amplifier-Based Current Compensator

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In the previously developed pure sinusoidal output single-phase current-source inverter (CSI), a conventional multilevel current-source inverter was successfully combined with a linear amplifier to realize a hybrid multilevel current-source inverter. Linear amplifier utilization was performed to reform a staircase multilevel current waveform into a pure sinusoidal current one by using a superimposition technique. To obtain very low harmonics by only using a small output filter capacitor, a class-A linear amplifier was utilized as the current compensator. However, this hybrid multilevel CSI must be applied in a high number of levels to achieve an acceptable power efficiency. Consequently, the system requires the use of many current modules that leads to a high semiconductor device count. Excessive semiconductor devices utilization, in turn, leads to performance deterioration due to switching and gate charge losses, and also decreases the power density of the system. Therefore, the recursive multilevel technique is proposed to handle the current module activation sequences, such that the high number of levels in the multilevel CSI can be constructed by only using a small number of current modules. The simulation and experimental results confirmed the applicability of the proposed technique with some advised discretions.

Keywords: single-phase, multilevel current-source inverter, superimposition, class-A linear amplifier, power efficiency, recursive multilevel

1. Introduction

The multilevel inverters become increasingly applied in industries especially for high-voltage transmission applications. These multilevel inverters commonly use voltage-source topologies, so that a high voltage can be generated by connecting each level in series [(1)(2)]. On the other hand, its dual circuit uses a current-source topology that enables the multilevel inverters to generate a high current by connecting all outputs of each level into one node, or notable as a parallel connection. Because of delivering only the current, it may neglect the fluctuation of the output voltage. Therefore, one of the applications which is suitable to use this topology is distributed power generation [(3)–(5)].

In the distributed power generation application, the DC power from renewable energy sources is fed into the grid through a grid connected inverter. Various international standards, such as IEEE-1547, IEEE-929 and EN-61000-3-2 impose some requirements for the inverter output, i.e. power quality. The harmonic currents and total harmonics distortion of the output current (THD-I) must be lower than specified limits in order to provide high quality electric power service [(3)–(5)]. The application of multilevel current-source inverters for the distributed power generation gives several advantages. Besides generating a low dv/dt or di/dt transient behavior, the multilevel technique also draws input current with very low distortion, and it is able to operate with low-switching frequency, so that the switching losses can be minimized [(6)–(9)].

Recently, a novel hybrid multilevel CSI system has been proposed by the authors [(10)–(13)]. The hybrid system incorporates a conventional multilevel current source inverter with a linear current generator. As shown in Fig. 1, the system consists of several current sources including a linear current generator, switching modules, and a polarity alternator represented by a CSI H-bridge circuit [(10)–(13)].

Figure 2 describes the basic operation principle of the hybrid system. The staircase multilevel current waveform is generated by the constant current sources controlled by the switching modules. While the linear compensating current is generated by a programmable linear current generator. The polarity alternator operates reversing the polarity of the load current every time a zero-crossing of the sinusoidal reference is detected. As a result, a pure sinusoidal current is generated by the system and is delivered to the load [(10)–(13)].

In order to simplify the circuit and to avoid using many dedicated current sources, a constant current source and a switching module are paired into one circuit called direct current module (DCM). Figure 3 shows the detailed circuit of

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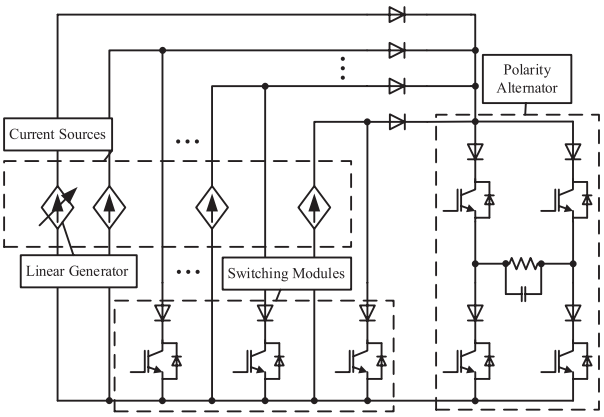


Fig. 1. Hybrid multilevel current-source inverter

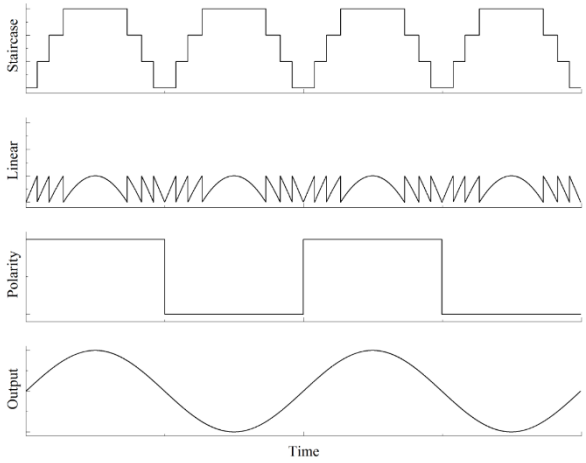


Fig. 2. Operation principle of the hybrid multilevel CSI

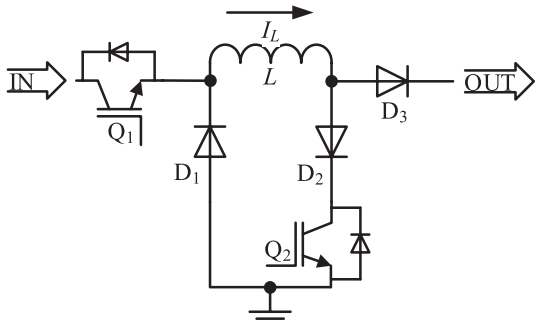


Fig. 3. Direct current module (DCM)

Table 1. DCM operation principle

Q1	Q2	Output
0	X[1]	0
Switching	0	I_L
X[1]	1	0

[1]X = do not care

the DCM that consists of Q1, D1, and L as parts of buck chopper-based constant current generator, with Q2, D2, and D3 as parts of switching module. The operation principle of this circuit is described in Table 1 [10)–(13)].

Due to simplification, the circuit in Fig. 1 is transformed into a circuit as shown in Fig. 4. By sharing a DC power source, all the DCM and the linear current generator con-

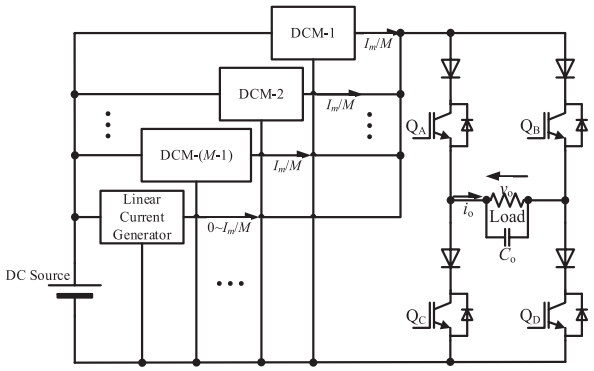


Fig. 4. Simplified hybrid multilevel CSI

tribute to generate a DC full-wave current in the DC link node. The H-bridge converts the direct current into an alternating current i_O by reversing its polarity every half period of the sinusoidal reference.

As i_O has a peak or the maximum amplitude value that equals to

$$I_m = \sqrt{2} i_O \quad \text{(A)}, \cdots\cdots (1)$$

each DCM and the linear current generator are subjected to generate a direct current with a maximum value that equals to

$$I_{CS} = \frac{I_m}{M} \quad \text{(A)}, \cdots\cdots (2)$$

where M is the number of required current sources that corresponds to the number of levels which is expressed by

$$M = \frac{N_{LEVEL} - 1}{2}. \cdots\cdots (3)$$

Equations (1)–(3) describe if a multilevel CSI system with 9-level configuration generates an alternating current of i_O, the system needs to employ 4 current sources which are composed of 3 DCMs and one linear current generator. Each DCM is programmed to generate a square wave current with an equal amplitude of I_{CS}, and the linear current generator is programmed to generate a linear current waveform with the maximum amplitude of I_{CS} as well. However, in order to generate a staircase multilevel current waveform, each square wave current generated by a DCM must have different duty cycle. The duty cycle of each square wave current is expressed by

$$D_n = 1 - \frac{2 \sin^{-1}\left(\frac{n}{M}\right)}{\pi}, \cdots\cdots (4)$$

where D_n is the duty cycle of the square wave current generated by DCM-n and M is the total number of current sources utilized in the system [10)(11)]. Figure 5 shows the basic staircase multilevel current waveform generation related to Fig. 2 with circuit configuration shown in Fig. 4, where the staircase multilevel current waveform is the summation of all square wave currents generated by all DCMs.

On the other hand, the linear compensating current is generated by subtracting the DC full-wave current reference with the generated staircase multilevel current. Figure 6 explains how the linear current waveform is generated [10)–(13)].

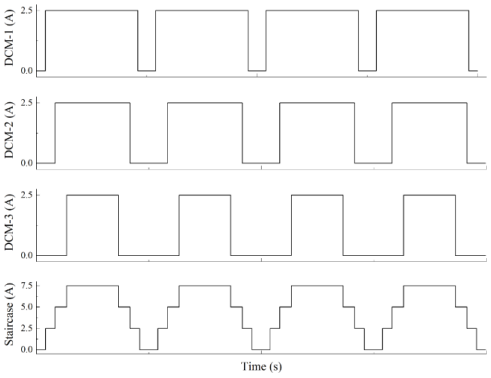


Fig. 5. Basic staircase multilevel current waveform generation

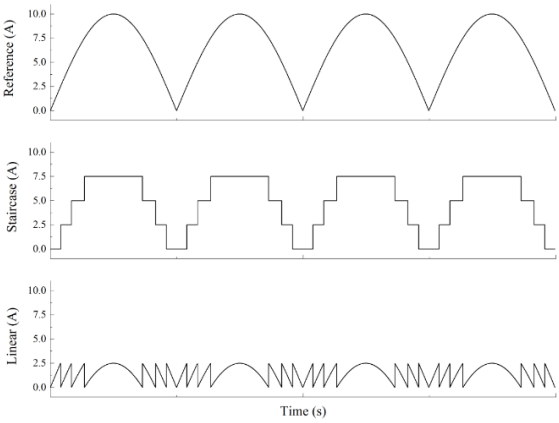


Fig. 6. Linear current waveform generation

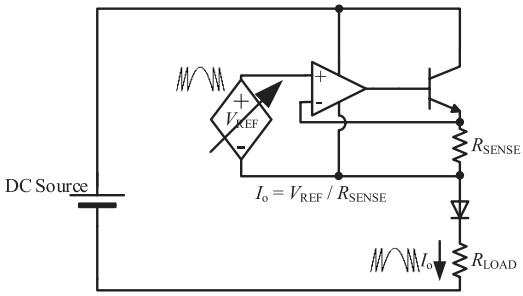


Fig. 7. Class-A amplifier-based linear current generator

Although this hybrid system has the following three main features: 1). No use of high-switching-frequency modulation for current inversion, 2). No use of a dedicated linear current amplifier, and 3). No use of a large output filter, it still has a flaw. Previous work reported that in order to generate a very low THD-I without using a large output capacitor, the system had to employ a class-A amplifier as a current compensator. Figure 7 shows the basic circuit of a class-A amplifier-based linear current generator that can function as a current compensator [10][12][13]. It consists of an operational amplifier, a power bipolar junction transistor, a current sense resistor, and a blocking diode. The circuit is configured as emitter follower so that the output current is the replica of its voltage reference. This class-A amplifier is well-known the most linear among all linear counterparts. However, its power efficiency is very substandard [14][15]. As a result, the power efficiency of the system was dragged down by this class-A amplifier circuit existence. In order to reduce the power loss, the amperage of linear compensating current must be as small as possible. To do that, according to Equation (2), the system should apply a high number of M, so that I_{CS} becomes small.

Unfortunately, if the system applies the high number of M, it must employ many DCMs. Because the number of DCMs is defined by

$$P = M - 1, \quad (5)$$

where P is number of DCMs and M is the number of utilized current sources in the system. As shown in Fig. 3, each DCM consists of five semiconductor devices and an inductor, excluding the supporting components. Instead of reducing the class-A amplifier power loss, the system dimension becomes larger. As a result, the power density of the system becomes low. The power efficiency might be decreased as well since the increment of switching and gate charge losses corresponds to the number of DCMs.

A possible solution to the problem at hand is applying a recursive multilevel technique. Recursive multilevel enables generating a small staircase multilevel current waveform inside the large staircase multilevel current waveform. Moreover, it is possible to generate a smaller staircase multilevel current waveform inside the small one and produce a multilayer staircase multilevel current generation. Because of this proposed current generation, one or more DCMs that are grouped for generating any sub-layer staircase multilevel current waveforms will be activated more than once or being switched by using multiplied fundamental frequency in accordance with the number of layers. As a result, a high number of levels staircase multilevel current waveform can be generated by using several DCMs and the required linear compensating current amplitude becomes smaller. Due to the smaller linear compensating current, the power efficiency is improved.

The present work is an extension of the work reported earlier by the author with an emphasis on reducing the DCM count in the hybrid multilevel CSI system without changing the number of levels. This work does not only give a significant advantage in reducing linear amplifier power loss, but also increases the power density of the system.

This paper is divided into five sections. Section 1 introduces the background, previous work, problems, proposed solution, objective, and significance of this research. Section 2 elaborates on the proposed operation principle and switching strategy. In order to verify the proper operation of the proposed system, several simulation and experimental results are presented in Section 3 and Section 4, respectively. Finally, Section 5 concludes the most important outcome of the work.

2. Proposed Operation Principle and Switching Strategy

2.1 Recursive Multilevel Recursive is an adjective form of recursion, where the definition of recursion itself is a method of solving a problem where the solution depends on solutions to smaller instances of the same problem. The recursive multilevel is also known as fractal multilevel [16].

There were only two literatures discuss a recursive method or similar approach for power inverters. The first literature

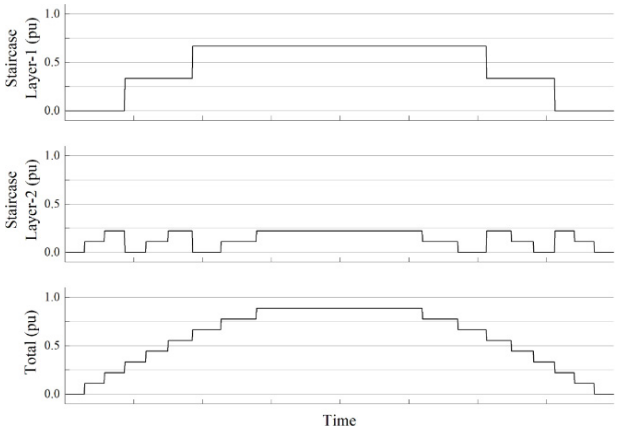


Fig. 8. Recursive multilevel

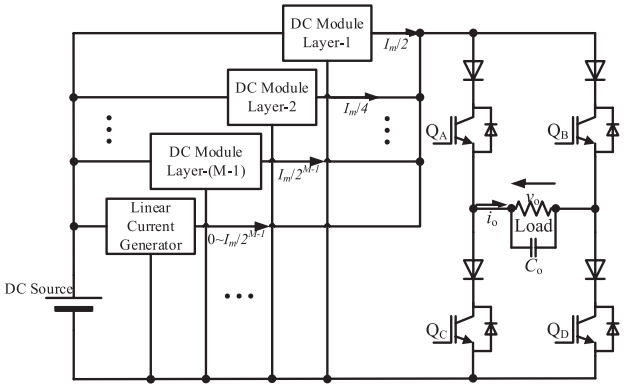


Fig. 9. Simplified implementation of recursive multilevel

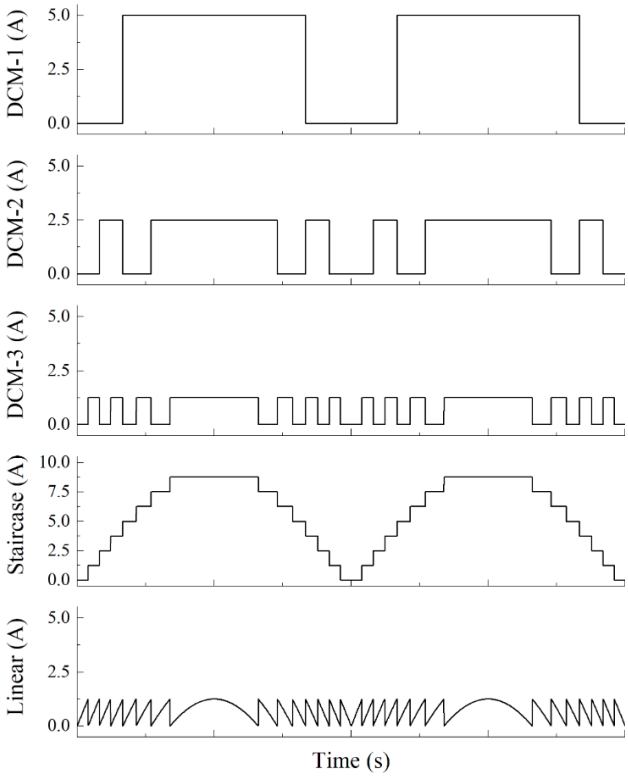


Fig. 10. Proposed operation principle by applying a recursive multilevel technique

was proposing an algorithm for n-level multi-point clamped voltage-source converter. The implementation was about the sub-hexagon space vector inside the main hexagon space vector modulation that is applied for the multilevel VSI [17]. The second one was proposing a modular asymmetric current feeder in order to reduce the count of the switch for multilevel current source inverter [18]. The implementation was about proposing a method to reduce switch count for a high number of levels of multilevel CSI. Despite having similar interests, this proposed method has a unique distinction that the recursive method is applied for the hybrid multilevel CSI system.

Figure 8 explains the example of the recursive multilevel application where the output staircase multilevel waveform can be generated by summing two staircase multilevel waveforms within different layers. The top waveform is the first layer 3-level staircase multilevel waveform with an amplitude of 2/3 per unit (pu). The second one is the second layer 3-level staircase multilevel waveform with the amplitude of 2/9 pu. The bottom one is the summation of all waveforms with a total amplitude of $2/3 + 2/9 = 24/27$ pu. It is shown that the 9-level staircase waveform can be generated by a recurring 3-level staircase waveform generation process.

2.2 Operation Principle In order to increase the number of levels without using additional current sources or DCMs, the staircase multilevel current waveform generation shown in Fig. 5 has to be modified. Figure 5 shows that each current source or DCM must have an equal current limit which is determined by Equation (2). On the other hand, the proposed method allows DCMs to have a different current limit in associated with the number of layers. The layer is defined by grouping the DCMs in terms of current limit settings. For instance, a given proposed system applies recursive multilevel with 3 layers staircase multilevel current generator and each layer uses one DCM as shown in Fig. 9. The simplest way to implement this method is by setting the current limit of the sub-layer DCM to half of the previous one. Thus, the first DCM current limit is set to generate a half of I_m, Meanwhile the next DCM current limit is set to generate a half of the previous one or $I_m/4$. This implementation is repeated until the last DCM utilized DCM [13].

Because of this rearrangement, each DCM generates a square wave current with different amplitude and frequency as shown in Fig. 10. If I_m is assumed to be 10 A, the top layer DCM generates a square wave current with an amplitude of $I_m/2$ or 5 A and two times the fundamental frequency. The second layer DCM generates a square wave current with an amplitude of $I_m/4$ or 2.5 A and six times the fundamental frequency. The third layer DCM generates a square wave current with an amplitude of $I_m/8$ or 1.25 A and 14 times the fundamental frequency.

As a result, the generated staircase multilevel current waveform has a characteristic of 8 stages, and the compensator is required to generate a linear current waveform with the maximum amplitude equal to the last layer DCM generated or $I_m/8$. To conclude, this operation principle indicates that a 17-level hybrid multilevel CSI can be constructed by using 3 DCMs and a linear compensator.

In Fig. 10, DCM-1 waveform indicates that the square

wave current is generated by using only one DCM in the first layer. For this reason, by referring to Equations (1)–(3) and Equation (5), M must be 2 and the average value of DCM-1 current waveform equals to $I_m/3$. In order to estimate the average square waveform value of the other layers, e.g. the DCM-2 square waveform as shown in Fig. 10, it must be broken down into odd square wave function and even square wave function as a consequence of being constructed by several square waveforms which nullify each other with different duty cycles. In other words, this is the opposite of the staircase waveform generation. The odd function of the square waveform generated by the recursive multilevel is expressed by

$$I_{ODD\_SQWAVE} = \frac{I_m}{\pi MN}\sum_{i=1}^{M}\left(\pi - 2\sin^{-1}\frac{2i-1}{MN}\right) \quad \text{(A)}, \qquad \cdots\cdots (6)$$

Meanwhile the even function one is expressed by

$$I_{EVEN\_SQWAVE} = \frac{I_m}{\pi MN}\sum_{i=1}^{M-1}\left(\pi - 2\sin^{-1}\frac{2i}{MN}\right) \quad \text{(A)}, \qquad \cdots\cdots (7)$$

where N is the division factor for the second layer. Owing to the amplitude of the current in this layer is half of the first layer and only one DCM is used, the value N must be 2. Hence, the average value of square waveform generated by second layer DCM can be written as

$$I_{DCM-2} = \frac{I_m}{\pi MN}\left[\sum_{i=1}^{M}\left(\pi - 2\sin^{-1}\frac{2i-1}{MN}\right) - \sum_{i=1}^{M-1}\left(\pi - 2\sin^{-1}\frac{2i}{MN}\right)\right] \quad \text{(A)} \cdots\cdots (8)$$

Similarly, the third layer generates the current with amplitude a half of second layer and using one DCM. Therefore, the equation for the average value of DCM-3 square waveform is expressed by

$$I_{DCM-3} = \frac{I_m}{\pi MNO}\left[\sum_{i=1}^{MN}\left(\pi - 2\sin^{-1}\frac{2i-1}{MNO}\right) - \sum_{i=1}^{MN-1}\left(\pi - 2\sin^{-1}\frac{2i}{MNO}\right)\right] \quad \text{(A)} \cdots\cdots (9)$$

where O is the division factor for the third layer. The factor must be 2 as well due to half current amplitude compared to the second one. Because of M, N, and O equal to 2, they can be substituted into the power of 2. As explained before that the staircase multilevel current waveform is the summation of all generated square waveforms. Therefore, the average value of the staircase multilevel current waveform generated by using the recursive multilevel technique can be defined by generalizing Equations (8) and (9) as follows

$$I_{STAIRCASE} = \frac{I_m}{\pi 2^L}\left[\sum_{i=1}^{2^{L-1}}\left(\pi - 2\sin^{-1}\frac{2i-1}{2^L}\right) - \sum_{i=1}^{2^{L-1}-1}\left(\pi - 2\sin^{-1}\frac{2i}{2^L}\right)\right] \quad \text{(A)} \cdots\cdots (10)$$

where L is the number of DCM layers applied in the system. Equation (10), however, only applies for the multilevel CSI system that employs the recursive multilevel technique with several layers and each layer only uses one DCM.

After the average value of staircase multilevel current waveform has been calculated, the average of linear compensating current can be found by subtracting the average value of DC full-wave reference current with generated staircase multilevel current that expressed by

$$I_{LINEAR} = \frac{2I_m}{\pi} - I_{STAIRCASE} \quad \text{(A)}. \cdots\cdots (11)$$

All these average value calculations have a function to estimate theoretical conduction loss of each current source. Hence, the total conduction losses of the system can be assessed [10][11].

2.3 Multilayer Stage Combination A new problem occurs when a high rating current application employs the recursive multilevel technique as shown in Fig. 10 [13]. Instead of reducing the number of current sources, the first layer DCM needs an enormous smoothing inductor that leads to the higher conduction loss and significantly reduces the system's power density. In order to solve this problem, the system must follow the basic concept of the recursive multilevel as shown in Fig. 8. To do this, the first layer must employ several DCMs that is sufficient to generate a desired high rating current with relatively small smoothing or energy buffer inductor. Due to this compromising design, a multilayer stage combination is introduced.

Multilayer stage combination enables the hybrid multilevel CSI designer to decide the most appropriate configuration that corresponds to the number of levels, output current rating, and physical dimension of the system. The configuration is basically determined by the current rating of the DCM. Sometimes, inductor size is also taken into account.

For instance, if each DCM has a current rating of 5 A, the multilevel CSI system with 30 A rating will need five DCMs for the first layer.

Because of this rule, the number of required DCMs for the first layer is expressed by

$$P_{LAYER\_1} = \frac{CSI\_current\_rating}{DCM\_current\_rating} - 1. \cdots\cdots (12)$$

The conventional configuration as shown in Fig. 4 is considered as the two-layer configuration or the minimum required layers. The first layer consists of three DCMs that generate the staircase multilevel current waveform and the second layer is occupied by the linear current compensator. On the other hand, the proposed configuration as shown in Fig. 9 is considered as the four-layer configuration in which each layer utilizes one current source. Thus, Fig. 4 and Fig. 9 represent the 3-1 and 1-1-1-1 multilayer stage combination, respectively.

Since the last layer is always utilizing a linear current compensator, in order to find the desired configuration, the last layer is excluded from the combination list and only the number of utilized DCMs is counted. The following table enlists several multilevel stage combination configurations that correspond to the number of utilized DCMs P in the multilevel CSI system. From Table 2, the number of combinations that

Table 2. Multilayer stage combination

Number of DCM (P)[1]	Number of DCM layers (L)	Possible configuration of DCMs in each layer (P_L)[2]
1	1	1
2	1	2
	2	1-1
3	1	3
	2	1-2 and 2-1
	3	1-1-1
4	1	4
	2	3-1, 2-2, and 1-3
	3	2-1-1, 1-2-1, and 1-1-2
	4	1-1-1-1
5	1	5
	2	4-1, 3-2, 2-3, and 1-4
	3	3-1-1, 1-3-1, 1-1-3, 2-2-1, 2-1-2, and 1-2-2
	4	2-1-1-1, 1-2-1-1, 1-1-2-1, and 1-1-1-2
	5	1-1-1-1-1

[1]The list shows until 5 DCMs utilization only.

[2]The layer for linear current compensator is excluded.

corresponds to the number of DCMs can be expressed as

$$MSC = 2^{P-1}, \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (13)$$

where MSC is total possible DCM configurations of the multilayer stage combination.

While the number of levels of the multilevel CSI applying recursive multilevel technique can be written as

$$N_{LEVEL} = 1 + 2\prod_{i=1}^{L}(P_i + 1), \cdots\cdots\cdots\cdots\cdots\cdots (14)$$

For instance, the given multilayer stage combination is 4-3-2 that consists of 9 DCMs which are grouped into 3 layers. 4 DCMs are on the first layer, 3 DCMs are on the second layer, and 2 DCMs are on the third layer. By using Equation (14), the number of levels is 121.

As explained beforehand, the proposed method allows DCMs having a different current limit in associated with the number of layers. The current limit or current reference for each layer is expressed by

$$I_{REF\_L} = \frac{I_m}{\prod_{i=1}^{L}(P_i + 1)} \quad \text{(A)}. \cdots\cdots\cdots\cdots\cdots\cdots (15)$$

Continuing the previous instance, if I_m is assumed to be 10 A, the current references for the layer-1, layer-2, and layer-3 are 2 A, 0.5 A, and 0.0167 A, respectively. The last layer is excluded due to linear current generator.

2.4 Control and Switching Strategy Since the proposed system only modifies the staircase multilevel current waveform generation, it uses a similar control scheme with the previous study. Due to recursive multilevel implementation, the DCM current controller must be multiplied in associate with the number of layers L. Figure 11 depicts the control system for the proposed hybrid multilevel CSI system. There are three types of close-loop controller used in the system, they are output voltage controller, inductor currents controller, and line frequency controller. For the voltage and current controlling, proportional-integrator controllers are used. While the line frequency controlling, a phase-locked loop (PLL) is used. From PLL, its phase data drives sinusoidal look-up table (LUT) and then the output of look-up table is considered as the sinusoidal waveform reference. The zero-crossing detector (ZCD) detects the zero-cross of the sinusoidal reference in order to reverse the polarity of the H-bridge. While the absolute value of the reference (i.e. full wave reference) is considered as the staircase multilevel current waveform reference as shown in Fig. 6. It is shown each reference current I_{REF} for the corresponding layer L is consecutively attenuated by M_L. Each attenuator M_L can be determined by

$$M_L = \prod_{i=1}^{L}(P_i + 1), \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (16)$$

While Fig. 12 shows the scheme of the proposed staircase multilevel current waveform generation applying the recursive multilevel technique which is referring to Fig. 8 operation principle. Each layer consists of two DCMs and $M_1 = M_2 = 3$. Hence, the first current limit of the layer-1 is 1/3 pu, the second current limit of the layer-1 is 2/3 pu, the first current limit of the layer-2 is 1/9 pu, and the second current limit of the layer-2 is 2/9 pu.

The output of each comparator switches the corresponding Q2 of the DCM circuit as shown in Fig. 3. When the reference exceeds the limit, Q2 is turned off to let the inductor current flowing to the load. When the reference goes down below the limit, Q2 is turned on to circulate the inductor current back to the chopper circuit.

Regarding the current limit, in the previous study subtractors took the reference from the same point of the first attenuator. On the other hand, in the proposed system the next layer subtractors take the reference from the first attenuator of each layer.

3. Simulation Results

In order to test the operation of the proposed hybrid multilevel CSI applying recursive multilevel, all possible configurations using four DCMs and a linear current compensator were simulated in PSIM. The simulation parameters are listed in Table 3.

According to Table 2, if the number of DCMs P is 4, then the possible combination is 8, they are 4, 3-1, 1-3, 2-2, 2-1-1, 1-2-1, 1-1-2 and 1-1-1-1. The combination of 4 DCMs in one layer is considered as the conventional 11-level configuration benchmark. This combination is shown in Fig. 13 where all DCMs are grouped into one ground line and each DCM generates the current with an equal limit. Figures 14, 15, and 16 show the combination of 3-1, 2-2, and 2-1-1, respectively. Their DCM current limit conforms to the designated configuration.

The simulation result of 2-2 combination or two-layer configuration with 2 DCMs in each layer is shown in Fig. 17 and its fast-Fourier-transform (FFT) harmonic analysis is shown in Fig. 18. These figures represent the recursive multilevel

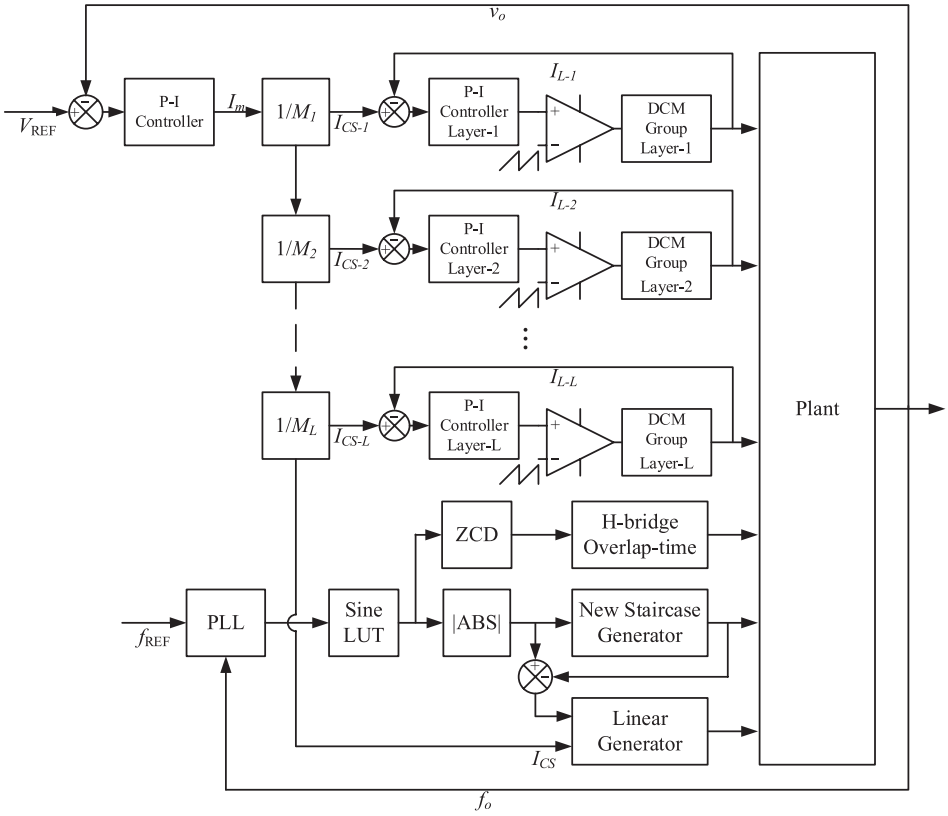


Fig. 11. Control scheme of the proposed hybrid multilevel CSI system

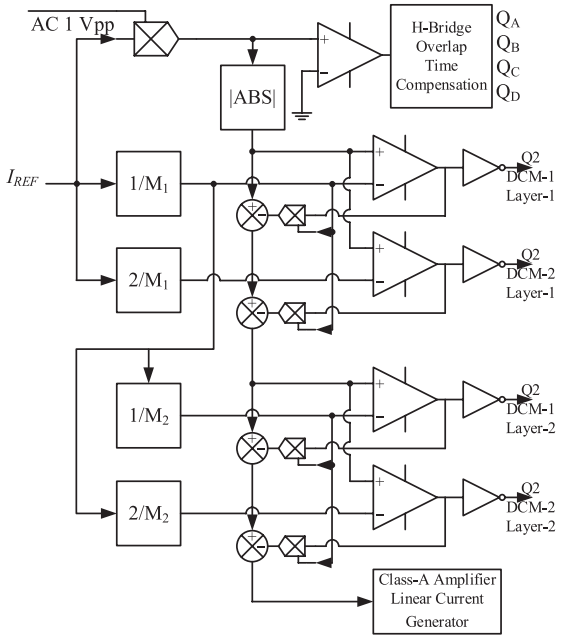


Fig. 12. Recursive staircase multilevel current waveform generation

Table 3. PSIM simulation parameters

Parameter	Value	Parameter	Value
Number of sources (M)	5	Bridge IGBT V_D/R_D	1.2 V/ 20 mΩ
Number of DCMs (P)	4	DCM blocking diodes	1.0 V/ 20 mΩ
DC voltage	160 V	Bridge blocking diodes	1.0 V/ 12.5 mΩ
Inductor	560 μH/ 0.09 Ω	Bipolar junction transistor h_{FE} gain	1000
Filter capacitor	6.8 μF/ 1 mΩ	Bipolar junction transistor bias/V_{CE} sat	5.0 V/ 1.0 V
Load	10 Ω/ 1 mH	Current sense resistor	1 Ω
DCM IGBT V_{CE}/R_E on	1.4 V/ 20 mΩ	Operational amplifier	Ideal
DCM IGBT V_D/R_D	1.0 V/ 20 mΩ	Sawtooth carrier frequency	50 kHz
Bridge IGBT V_{CE}/R_{E_ON}	1.8 V/ 20 mΩ	Output voltage	100 V/ 60 Hz

technique implementation. The measured quantities of all configuration are reported in Table 4.

Figures 13–16 show the resultant of the current limit always equals to I_m. Based on Equation (14), one-layer 4 DCMs generates the 11-level hybrid multilevel CSI. While 3-1, 2-2, and 2-1-1 configurations generate 17-level, 19-level, and 25-level hybrid multilevel CSI, respectively.

Figure 17 shows the operational simulation result of the proposed 19-level hybrid multilevel CSI applying the recursive multilevel technique with a multilayer stage combination of 2-2 using 4 DCMs. The top waveform is the load voltage. The second waveform is the load current before filtering. The third and fourth waveforms are the staircase multilevel currents of the first layer and the second layer, respectively. And the last waveform is the linear compensating current. It is shown the unfiltered load current is the summation of stair-

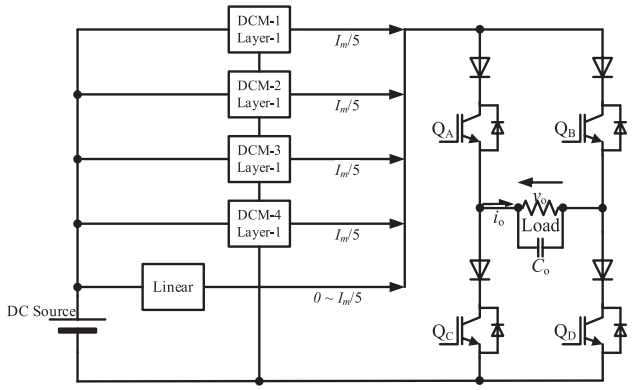


Fig. 13. Conventional or one-layer 4 DCMs configuration

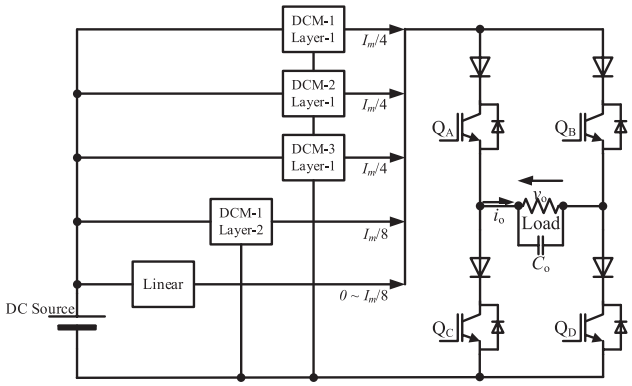


Fig. 14. Two-layer 3-1 DCMs configuration

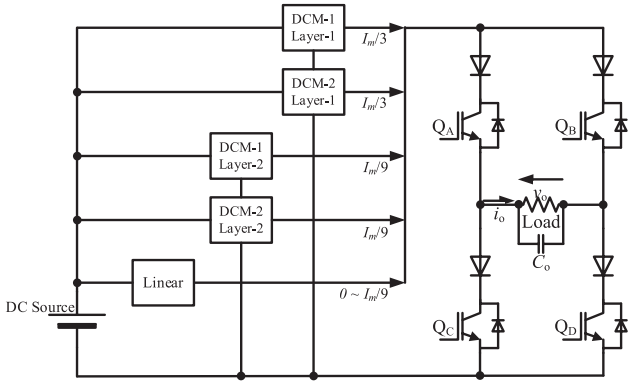


Fig. 15. Two-layer 2-2 DCMs configuration

case layer-1, staircase layer-2, and the linear with polarity reversal assistance. This simulation result has proven the proposed recursive multilevel technique application is eligible to generate a 19-level current waveform by only using 4 DCMs.

Figure 18 describes the FFT analysis of the unfiltered load current and the load voltage. The horizontal axis is the harmonic spectrum frequency from 0 Hz to 60 kHz, meanwhile the vertical axis is the normalized harmonic amplitude to the logarithmic unity in percent. Prior to filtering process, the total load current harmonics were approximately 4%. By using 6.8 μF output filter capacitor, these harmonics were successfully attenuated. As a result, the THD-V was only around 2%. Hence, the generated output voltage waveform conforms to the various international standards.

Table 4 reported all PSIM simulation measured quantities which are important to be discussed. The conventional con-

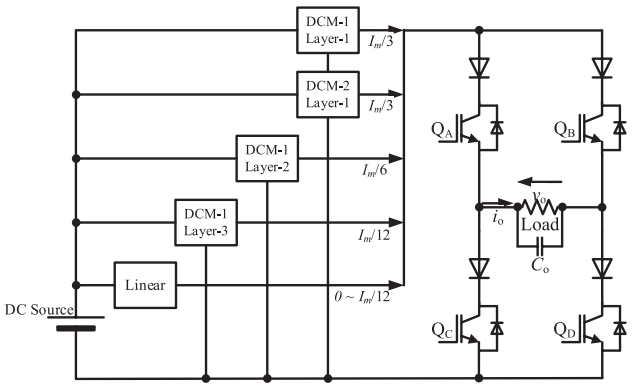


Fig. 16. Three-layer 2-1-1 DCMs configuration

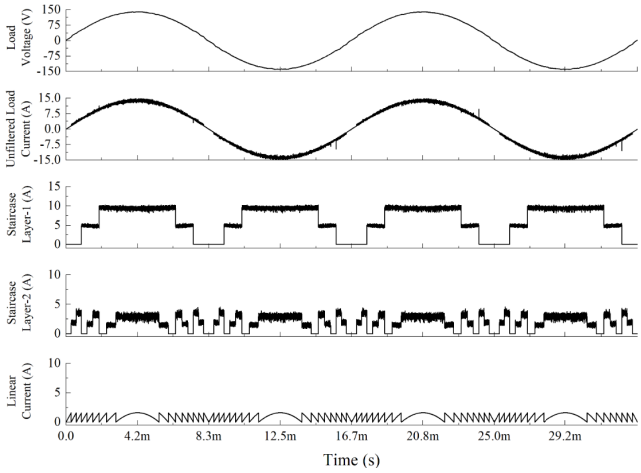


Fig. 17. Two-layer 2-2 DCMs configuration simulation result

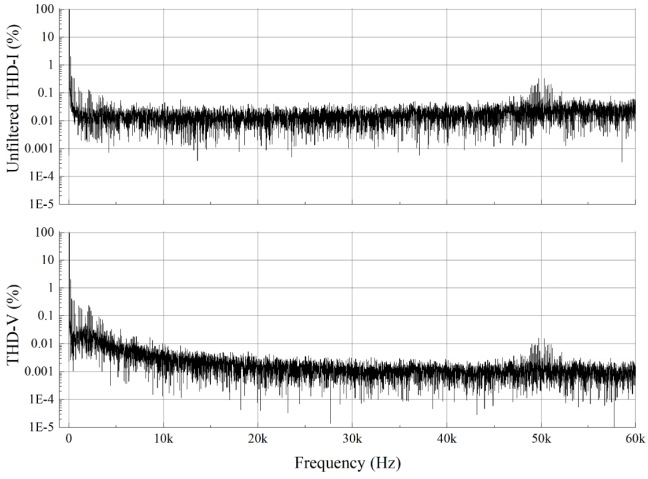


Fig. 18. FFT analysis of unfiltered load current and the load voltage of two-layer 2-2 DCMs configuration

figuration only brought the power efficiency out of 83.9% with an 11-level multilevel current waveform. While the recursive multilevel implementation with DCM multilayer stage combination of 2-1-1 gave 87.1% with a 25-level one. These results confirmed that the proposed method did not only enhance the power density, but also the power efficiency. However, the harmonics were slightly increased. Since the THD values did not exceed the international standards' limit, the proposed system with a multilayer stage combination of

Table 4. PSIM measured quantities

	Multilayer Stage Combination of 4 DCMs			
	4[1]	3-1	2-2	2-1-1
Number of levels	11	17	19	25
AC load current (A)	9.99	9.99	9.99	9.99
AC load voltage (V)	100.0	100.0	100.0	100.0
DC source current (A)	7.43	7.25	7.24	7.16
THD-I (%)	2.05	2.18	2.30	2.40
THD-V (%)	2.15	2.28	2.39	2.48
Unfiltered THD-I (%)	3.76	3.68	3.85	3.67
Power efficiency (%)	83.9	86.0	86.2	87.1

[1]Conventional configuration.

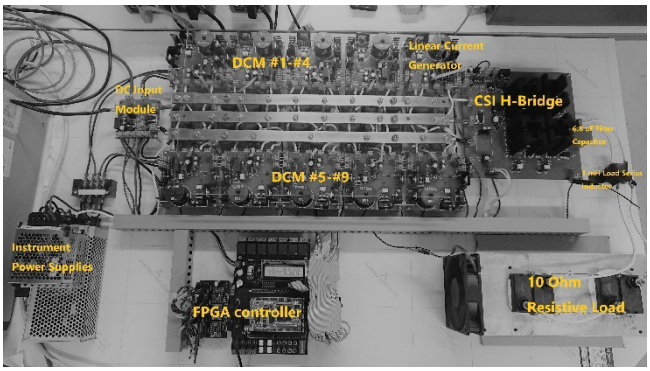


Fig. 19. Experimental setup

2-1-1 configuration was considered giving the best simulation performance.

4. Experimental Results

In order to validate the simulation results, configurations shown in Figs. 13–16 were implemented on an experimental setup. A laboratory prototype has been constructed that consisted of 9 DCMs, a programmable linear current generator, a CSI H-bridge module, a DC input module, instrument power supplies, and dummy loads. For the DCM circuit, IGBT STGP20V60DF from ST Microelectronics was used as the switches and SiC Schottky diode CREE C3D10060A from Wolfspeed was used as the freewheeling and blocking diodes. The CSI H-bridge module used IGBT STGW60V60DF from ST Microelectronics as switches and ultra-fast recovery diode STTH60RQ06 from ST Microelectronics as the blocking diodes. The programmable linear current generator utilized 5 Ampere adjustable regulator IC LM338T from Texas Instruments with a high-voltage protection circuit that composed of several bipolar junction transistor BU941ZT from ST Microelectronics and zener diode 1N5366B from Micro Commercial. For the main controller, an FPGA Xilinx Kintex-7 was utilized. The complete hardware experimental setup is shown in Fig. 19. While the measurement instruments utilized Yokogawa DL850E ScopeCorder for the oscilloscope and Yokogawa WT1800 as the power analyzer.

It is reasonable that a number of limitations might have influenced the results obtained. Due to limited literature about CSI hardware implementation, the prototype seemed not optimized. As shown in Fig. 19, the currents from each DCM were delivered to the CSI H-Bridge via copper bus bars. Even though using large bus bars, there were some different output wire lengths between one DCM with the others that resulted in various conduction losses on each branch. This design lack of unequal wire length was not expected before. However, the setup has already been constructed and the experiments must still be conducted.

The first experiment was carried out by implementing a conventional configuration that consists of one-layer 4 DCMs and a linear current generator. This configuration experimental results were considered as the benchmark or the reference for the other configurations. The results are shown in Figs. 20(a) and 20(b). Figure 20(a) shows various output waveforms that consist of staircase multilevel current, linear compensating current, unfiltered load current, and load voltage. While Fig. 20(b) shows the FFT analysis of unfiltered load current and load voltage.

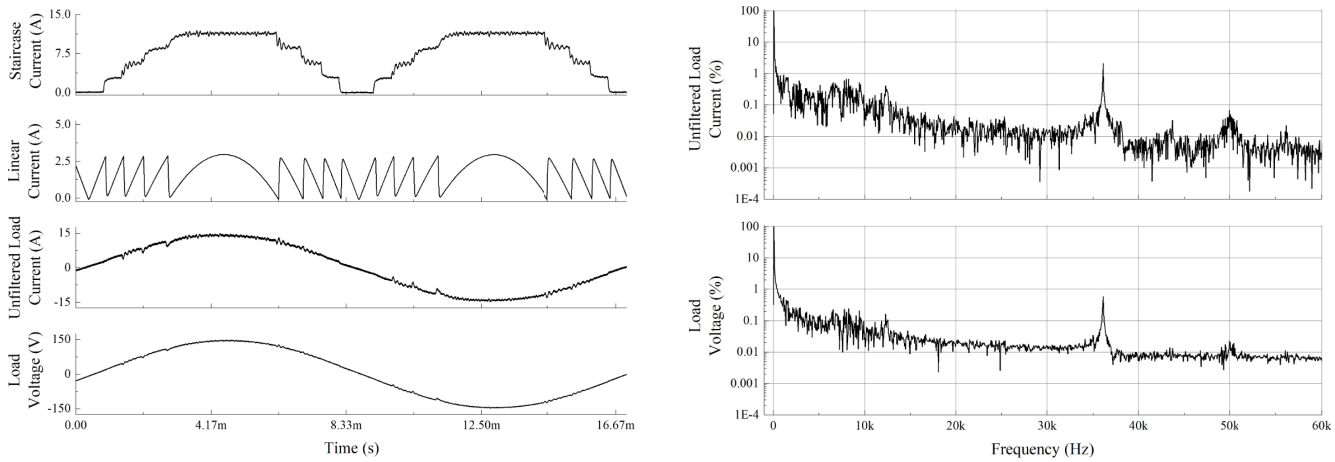
The proposed method experiments were carried out by implementing two-layer 3-1 and 2-2 DCMs configurations, and three-layer 2-1-1 DCMs configuration. The results are shown in Figs. 21, 22 and 23, respectively. Figures 21(a), 22(a), and 23(a) show various output waveforms that consist of multilayer staircase multilevel currents, linear compensating current, unfiltered load current, and load voltage for the respective configurations. While Figs. 21(b), 22(b), and 23(b) show the FFT analysis of the unfiltered load current and the load voltage of the respective configurations.

Figures 21(a), 22(a), and 23(a) show the confirmation of the proposed method is applicable to be realized. However, there are some findings obtained from these experimental results. Compared to the conventional configuration results as depicted in Fig. 20(a), the output voltage noises were increasing in accordance with the number of levels. This first finding is in line with the simulation results that by using a small number of current sources, constructing a system with a high number of levels will degrade the output power quality.

The second findings were highlighted from their FFT analysis that the harmonic spectrum contributed by the buck chopper switching frequency was shifted from 50 kHz to around 36 kHz. It did not occur in every single simulation result and only occurred in experimental results. Figures 20(b), 21(b), 22(b), and 23(b) indicated this shifting. These were caused by unoptimized prototype design when mixing the constant current generated by buck choppers with the linear current generated by the class-A amplifier circuit.

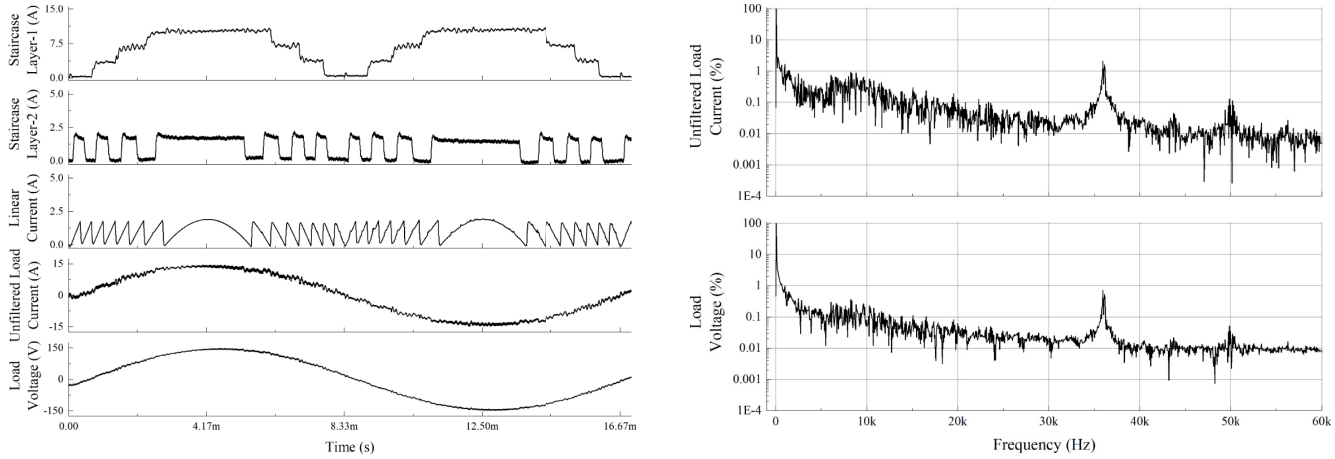
The measured power efficiency of the conventional configuration, two-layer 3-1 and 2-2 DCMs configurations, and three-layer 2-1-1 DCMs configuration are 89.1%, 90.1%, 90.6%, and 91.6%, respectively. While the measured output voltage harmonics of each configuration are 3.20%, 3.75%, 4.25%, and 4.80%, respectively. It is confirmed the proposed method can increase at least 2.5% power efficiency experimentally while using five current sources. This power efficiency result could be better if using more than a demonstrated setup. However, the harmonic measurement results have not given a free-will configuration selection. Hence, in order to construct optimal system, the application of the proposed method must consider not only the power efficiency and the power density, but also the power quality.

In order to compare between the simulation and the experimental results, Fig. 24 is presented. It is shown that the



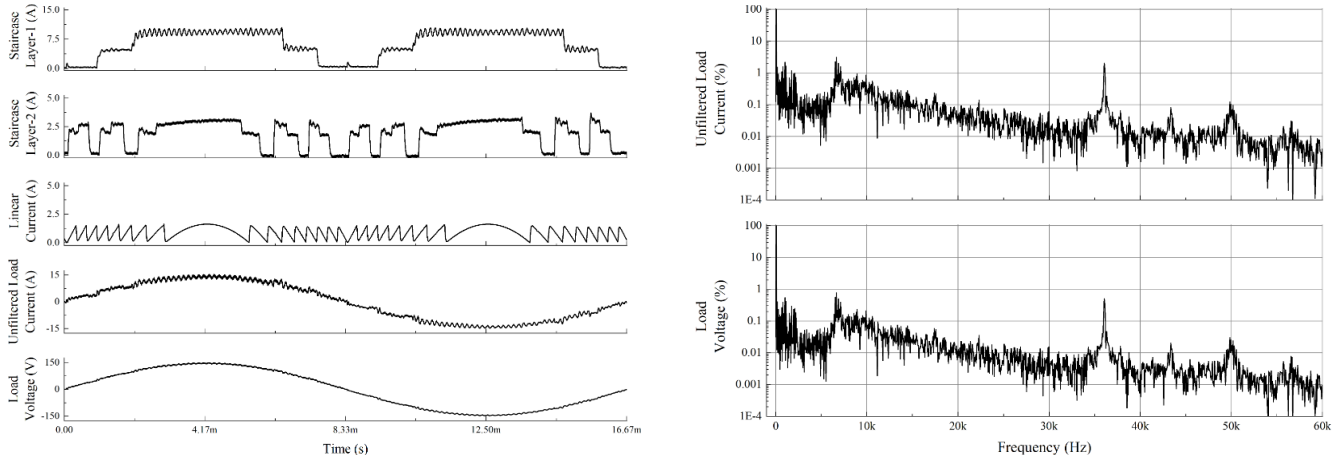
(a) (b)

Fig. 20. Conventional configuration experimental results: a). Output waveforms, b). FFT analysis of unfiltered load current and load voltage



(a) (b)

Fig. 21. Recursive multilevel, 3-1 DCMs configuration experimental results: a). Output waveforms, b). FFT analysis of unfiltered load current and load voltage



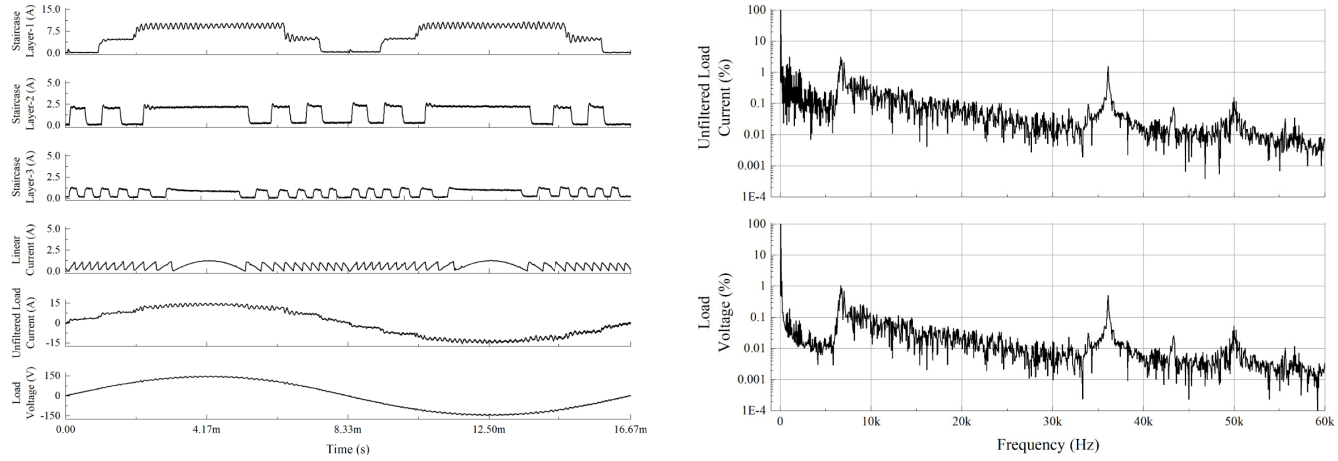
(a) (b)

Fig. 22. Recursive multilevel, 2-2 DCMs configuration experimental results: a). Output waveforms, b). FFT analysis of unfiltered load current and load voltage

experimental power efficiency results seemed linear to the simulation power efficiency results with small difference. On the other hand, the load voltage harmonic results have a large gap due to prototype design lack.

5. Conclusions

An advanced method for increasing the power efficiency and the power density of the pure sinusoidal output



(a) (b)

Fig. 23. Recursive multilevel, 2-1-1 DCMs configuration experimental results: a). Output waveforms, b). FFT analysis of unfiltered load current and load voltage

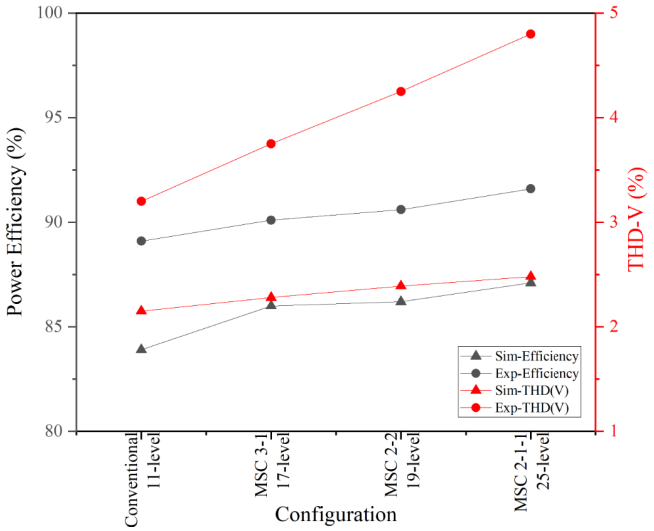


Fig. 24. Simulation vs experimental results

single-phase multilevel current-source inverter employing class-A linear current compensator with reduced number of current sources has been confirmed by both simulation and experimental results.

By applying the recursive multilevel approach, it is possible to construct a high number of levels multilevel CSI with small number of current sources. As a result, the power density of the multilevel CSI is increased.

Besides improving the power density, both simulation and experimental results have confirmed the recursive multilevel can improve the system power efficiency as well. Due to high number of levels, the required linear compensating current is smaller. As a result, the linear amplifier power loss is greatly reduced.

However, the power efficiency enhancement does not show a very significant result while using a small number of current sources. Enlarging the number of levels with a small number of current sources is not recommended because it will degrade the power quality of the system.

In order to construct an optimal system, the multilevel stage combination has provided alternative configurations by considering not only the power efficiency and the power density, but also the power quality. Therefore, system designer discretion while choosing proper configuration is advised.

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